



Call for Papers

IEEE/ACM INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN
November 2-5 2020 • San Diego Mission Bay Resort, San Diego, CA 92109 • ICCAD.com

ORIGINAL TECHNICAL SUBMISSIONS ON, BUT NOT LIMITED TO, THE FOLLOWING TOPICS ARE INVITED:

1) SYSTEM-LEVEL CAD

1.1 System Design

- System-level specification, modeling, and simulation
- System design flows and methods
- HW/SW co-design, co-simulation, co-optimization, and co-exploration
- HW/SW platforms for rapid prototyping
- HW/SW prototyping and emulation on FPGAs
- System-level design case studies and applications
- System-level issues for 3D integration
- Analysis and optimization of data centers
- Micro-architectural transformation
- Memory architecture and system synthesis
- System communication architecture
- Network-on-chip design methodologies
- Modeling and simulation of heterogeneous platforms
- High-level synthesis for heterogeneous computing
- Power/performance analysis of heterogeneous platforms
- Programming environment of heterogeneous computing
- Application driven heterogeneous platforms for big data, machine learning etc.
- Applications and designs for systems based on optical devices

1.2 Embedded Systems, Cyber-physical Systems (CPS) and Internet-of-Things (IoT)

- HW/SW co-design for embedded systems
- Multi-/Many-core processor, GPU and heterogeneous SoC for embedded systems
- Static and dynamic reconfigurable architectures
- Domain-specific accelerators
- Memory hierarchies and management
- System-level consideration of custom storage architectures
- Energy/power management and energy harvesting
- AI and machine learning for embedded systems
- CAD for IoT
- Security, privacy, reliability for IoT
- Edge and fog computing
- Modeling and analysis of CPS systems
- Dependable, safe, and secure CPS systems design
- Green computing (smart grid, energy, solar panels, etc.)
- CAD for application domains including wearables, health care, autonomous systems, smart cities

1.3 Neural Networks and Deep Learning

- Hardware and architecture for neural networks
- Compilers for deep neural networks
- Design method for learning on a chip
- System-level design for (deep) neural computing
- Neural network acceleration techniques including GPGPU, FPGA and dedicated ASICs
- Safe and secure machine learning
- Hardware accelerators for Artificial Intelligence

1.4 Neuromorphic Computing

- Network and neuron models
- Devices and hardware implementations
- Non-von Neumann architectures
- Event or spike-based hardware systems
- CAD for bio-inspired and neuromorphic systems

1.5 Embedded Software

- Real-time software and operating systems
- Scheduling and execution time analysis
- Middleware, virtual machines, runtime support, and resource management

- Profiling and compilation techniques
- Software synthesis, testing, validation, verification, and optimization
- Software design for multicores, GPUs, and heterogeneous embedded architectures
- Software for safe autonomy
- Energy-efficient embedded software

1.6 Hardware Security

- Hardware Trojans, side-channel attacks, fault attacks and countermeasures
- Detection and prevention of hardware Trojans
- New physical attack vectors or methods for ASICs and FPGAs
- Nanoelectronic security
- Hardware-based security (CAD for PUF's, RNG, AES etc.)
- Artificial Intelligence for attack prevention systems
- Design and CAD for security
- Security implications of CAD

1.7 Security Architecture and System

- Embedded software forensics
- Embedded software security
- Trustworthy embedded software
- Trusted execution environments
- Cache-side channel attack and mitigation
- Privacy-preserving computation
- Cloud Computing data security
- Internet-of-Things security
- Automotive/autonomous system security
- FPGA and reconfigurable fabric security
- Sensor network security
- Split Manufacturing for security
- Supply chain security and anti-counterfeiting

1.8 Low Power and Approximate Computing in System Design

- Power and thermal estimation, analysis, optimization, and management techniques for hardware and software systems
- Energy- and thermal aware application mapping and scheduling
- Energy- and thermal-aware architectures, algorithms, techniques
- Energy- and thermal-aware dark silicon system design and optimization
- Run-time management for the dark silicon
- New hardware techniques for approximate/stochastic computing

2) SYNTHESIS, VERIFICATION, AND PHYSICAL DESIGN

2.1 High-Level, Behavioral, and Logic Synthesis and Optimization

- High-level/Behavioral/Logic synthesis
- Technology-independent optimization and technology mapping
- Functional and logic timing ECO
- Resource scheduling, allocation, and synthesis
- Interaction between logic synthesis and physical design

2.2 Testing, Validation, Simulation, and Verification

- High-level/Behavioral/Logic modeling and validation
- High-level/Behavioral/Logic simulation
- Formal, semi-formal, and assertion-based verification
- Equivalence and property checking
- Emulation and hardware simulation/acceleration
- Post-silicon functional validation
- Digital fault modeling and simulation
- Delay, current-based, low-power test
- ATPG, BIST, DFT, and compression
- Memory test and repair
- Core, board, system, and 3D IC test
- Post-silicon validation and debug
- Analog, mixed-signal, and RF test



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2.3 Cell-Library Design, Partitioning, Floorplanning, Placement

- Cell-library design and optimization
- Transistor and gate sizing
- High-level physical design and synthesis
- Estimation and hierarchy management
- 2D and 3D partitioning, floorplanning, and placement
- Post-placement optimization
- Buffer insertion and interconnect planning
- Post-synthesis optimization for FPGAs

2.4 Clock Network Synthesis, Routing, and Post-Layout Optimization and Verification

- 2D and 3D clock network synthesis
- 2D and 3D global and detailed routing
- Package-/Board-level routing and chip-package-board co-design
- Post-layout/-silicon optimization
- Layout and routing issues for optical interconnects

3) SOC ANALYSIS, DESIGN, SIMULATION, AND TESTING

3.1 Design for Manufacturability and Design for Reliability

- Process technology characterization, extraction, and modeling
- CAD for design/manufacturing interfaces
- CAD for reticle enhancement and lithography-related design
- Variability analysis and statistical design and optimization
- Yield estimation and design for yield
- Physical verification and design rule checking
- DFM for emerging devices (3D, nanophotonics, non-volatile logic/memory, etc.)
- Machine learning for smart manufacturing and process control
- Analysis and optimization for device-level reliability issues (stress, aging effects, ESD, etc.)
- Analysis optimization for interconnect reliability issues (electromigration, thermal, etc.)
- Reliability issues related to soft errors
- Design for resilience and robustness
- Reliability issues for emerging devices (3D, optical, non-volatile, etc.)

3.2 Timing, Power and Signal Integrity Analysis and Optimization

- Deterministic and statistical static timing analysis and optimization
- Power and leakage analysis and optimization
- Circuit and interconnect-level low power design issues
- Power/ground network analysis and synthesis
- Signal integrity analysis and optimization

3.3 CAD for Analog/Mixed-Signal/RF and Multi-Domain Modeling

- CAD for analog, mixed-signal, RF
- CAD for mixed-domain (semiconductor, nanoelectronic, MEMS, and electrooptical) devices, circuits, and systems
- CAD for nanophotonics and optical devices
- FPGA-based prototyping for analog, mixed-signal, RF systems
- Analog, mixed-signal, and RF noise modeling and simulation
- Device, interconnect and circuit extraction and simulation
- Package modeling and analysis
- EM simulation and optimization
- Behavior modeling of devices and interconnect
- Modeling of complex dynamical systems (molecular dynamics, fluid dynamics, computational finance, etc.)

4) CAD FOR EMERGING TECHNOLOGIES, PARADIGMS, AND APPLICATIONS

4.1 Biological Systems and Electronics, Brain Inspired Computing, and New Computing Paradigms

- CAD for biological computing systems
- CAD for systems and synthetic biology
- CAD for bio-electronic devices, bio-sensors, MEMS, and systems

4.2 Nanoscale and Post-CMOS Systems

- New device structures and process technologies
- New memory technologies (flash, phase change memory, STT-RAM, memristor, etc.)
- Nanotechnologies, nanowires, nanotubes, graphene, etc.
- Quantum computing
- Optical devices, computing, and communication

SUBMISSION DETAILS

Paper submissions must be made through the online submission system at the ICCAD web site: <https://www.softconf.com/i/ccad2020>.

Regular papers will be reviewed as finished papers; preliminary submissions will be at a disadvantage. Research papers accompanied by open-source software are encouraged.

Authors are asked to submit their work in two stages. In stage one (abstract submission), a title, abstract, and a list of all co-authors must be submitted via the ICCAD web submission site. In stage two (paper submission), the paper itself is submitted whereby the submitted abstract of stage one can still be modified. Authors are responsible for ensuring that their paper submission meets all guidelines, and that the PDF is readable.

DEADLINE FOR ABSTRACT SUBMISSIONS

The submission abstract deadline is 5:00pm PDT (GMT -07:00) **Thursday, May 21, 2020**. No abstract submissions will be possible after this deadline.

DEADLINE FOR PAPER SUBMISSIONS

The submission deadline for paper is 5:00pm PDT (GMT -07:00) **Thursday, May 28, 2020**.

We always have several authors contact the ICCAD office asking for a deadline extension. Due to the limited review cycle, NO extensions will be granted for ANY reason.

REGULAR PAPER SUBMISSIONS

- All papers must be in PDF format only, with savable text and embedded fonts in included (vector) graphics.
- Each paper must be no more than 8 pages (including the abstract, figures and tables), double-columned, 9pt or 10pt font. Starting from this year, one page of references is allowed, which does not count towards this 8-page limitation.
- Your submission must not include information that serves to identify the authors of the manuscript, such as name(s) or affiliation(s) of the author(s), anywhere in the manuscript, abstract, or in the embedded PDF data. References and bibliographic citations to the author(s) own published works or affiliations should be made in the third person.
- Submissions not adhering to these rules, or determined to be previously published or simultaneously submitted to another conference, or journal, will be summarily rejected. Internal memoranda with full content not publicly available, and with author names not divulged, may be submitted.



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IMPORTANT: Final camera-ready versions must be identical to the submitted papers with the following exceptions; inclusion of author names/affiliation, correction of identified errors, addressing reviewer-demanded changes. No other modifications of any kind are allowed including modification of title, change of the author list, reformatting, restyling, rephrasing, removing figures/results/text, etc. The TPC Chairs reserve the right to finally reject any manuscripts not adhering to these rules. A report detailing all the revisions made must be submitted together with the final camera-ready manuscript once any revision is conducted.

TEMPLATES

Paper templates are available at the ICCAD website and authors are recommended to format their papers based on the ACM template.

NOTIFICATION OF ACCEPTANCE

Authors will be notified of acceptance on or before [Tuesday, July 21, 2020](#). Final paper guidelines will be sent at that time.

PROCEEDINGS

The deadline for final papers is [Friday, August 14, 2020](#). Accepted regular papers are allowed six pages plus one page of references in the conference proceedings free of charge. Each additional page (except references) beyond six pages is subject to the page charge at \$150.00 per page up to the eight-page plus one page of references. ACM will hold the copyright for ICCAD 2020 proceedings. Authors of accepted papers must sign an ACM copyright release form for their paper.

CONFERENCE REGISTRATION

At least one author per accepted regular paper or poster must register by [Monday, August 17, 2020](#), at the discounted speaker's registration rate. Failure to register will result in your paper being removed from the conference proceedings. In case of a regular paper, ACM reserves the right to exclude a paper from distribution after the conference (e.g., removal from IEEE Xplore) if the paper is not presented at the conference. Starting from this year, the presentation of a regular paper includes both an oral **and** a poster presentation. The mandatory poster presentation will, in addition to the regular oral presentation, further stimulate the technical discussions.

ACM/IEEE WILLIAM J. MCCALLA ICCAD BEST PAPER AWARD

The awards are split into three categories. Two papers from this year's ICCAD conference, one from front-end and one from back-end, will be awarded with this prestigious award. The winners will be chosen from nominated papers after a thorough and competitive process by area-specific selection committees and announced at the opening session.

ICCAD TEN-YEAR RETROSPECTIVE MOST INFLUENTIAL PAPER AWARD

One paper from the 2010 and 2011 editions of ICCAD will be selected for the 10-year retrospective most influential paper award as evidenced by impact on the research community reflected in citations, on the vendor community via its use in an industrial setting, or by initiating new research venues during the past decade. Nominations from the community are welcome and can be sent to Tulika Mitra, Technical Program Vice Chair at tulika@comp.nus.edu.sg.

Call for Workshop, Tutorial, Special Session, Panel and Keynote Proposals are all due on [Thursday, May 28, 2020](#).

CALL FOR PROPOSALS

WORKSHOP PROPOSALS

ICCAD provides a vibrant and supportive environment for small-to-medium-sized affiliated workshops. Typical workshops are one-day events on the Thursday of ICCAD, with ICCAD providing all logistical support (registration, lunch, room bookings, hotel, pre-conference financials, etc.) All workshop proposals should be submitted through the ICCAD website or sent to, Workshop Chair Jinjun Xiong, at jinjun@us.ibm.com.

TUTORIAL PROPOSALS

All ICCAD tutorials are embedded in the main technical program and free to conference attendees, providing value to attendees and a good audience for presenters. Typical tutorials run 1.5-2 hours, although longer tutorials (consisting of two session blocks of 1.5-2 hours each) may be considered. Tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants with biographical data. Proposals should focus on the state-of-the-art in a specific area of broad interest amongst ICCAD attendees. All tutorial proposals should be submitted through the ICCAD website or sent to Evangeline Young, Tutorial and Special Sessions Chair, at fyyoung@cse.cuhk.edu.hk.

SPECIAL SESSION PROPOSALS

Special Sessions typically run 1.5-2 hours. Special session proposals should focus on in-depth treatment on a topic of timely interest to the ICCAD audience. Special session proposals should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants with biographical data. All special session proposals should be submitted through the ICCAD website or sent to Evangeline Young, Tutorial and Special Sessions Chair, at fyyoung@cse.cuhk.edu.hk.

PANEL PROPOSALS

Panel suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Panel suggestions must include a bulleted outline of covered topics. All panel proposals should be sent to Rolf Drechsler, Program Chair at drechsler@uni-bremen.de.

KEYNOTE PROPOSALS

Keynote proposals should include descriptions of suggested keynote speakers, and the importance of the speech to the ICCAD audience. All keynote proposals should be sent to Yuan Xie, General Chair, at yuanxie@ece.ucsb.edu.

ICCAD reserves the right to restructure all panel, special session, and tutorial proposals.

IF YOU NEED ASSISTANCE, PLEASE CONTACT THE APPROPRIATE COMMITTEE MEMBERS

General Chair: Yuan Xie, yuanxie@ece.ucsb.edu

Program Chair: Rolf Drechsler, drechsler@uni-bremen.de

Vice Program Chair: Tulika Mitra, tulika@comp.nus.edu.sg

Tutorial and Special Session Chair: Evangeline Young, fyyoung@cse.cuhk.edu.hk

Workshop Chair: Jinjun Xiong, jinjun@us.ibm.com

