<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Welcome Message</td>
<td>2</td>
</tr>
<tr>
<td>General Information</td>
<td>4</td>
</tr>
<tr>
<td>CADathlon at ICCAD</td>
<td>6</td>
</tr>
<tr>
<td>Sunday Workshops</td>
<td>7</td>
</tr>
<tr>
<td>Best Paper Candidates &amp; Committees</td>
<td>9</td>
</tr>
<tr>
<td>Monday Schedule</td>
<td>10</td>
</tr>
<tr>
<td>Opening Session &amp; Award Presentations</td>
<td>12</td>
</tr>
<tr>
<td>Monday Keynote Address</td>
<td>13</td>
</tr>
<tr>
<td>Monday Session Details</td>
<td>14</td>
</tr>
<tr>
<td>ACM Student Research Competition Poster Session</td>
<td>18</td>
</tr>
<tr>
<td>ACM Student Research Competition Technical Presentations</td>
<td>27</td>
</tr>
<tr>
<td>Tuesday Schedule</td>
<td>28</td>
</tr>
<tr>
<td>Tuesday Session Details</td>
<td>30</td>
</tr>
<tr>
<td>Tuesday Invited Keynote Luncheon</td>
<td>36</td>
</tr>
<tr>
<td>ACM/SIGDA Membership Meeting</td>
<td>45</td>
</tr>
<tr>
<td>Wednesday Schedule</td>
<td>46</td>
</tr>
<tr>
<td>Wednesday Keynote Address</td>
<td>48</td>
</tr>
<tr>
<td>Wednesday Session Details</td>
<td>49</td>
</tr>
<tr>
<td>Thursday Schedule</td>
<td>60</td>
</tr>
<tr>
<td>Thursday Workshop Details</td>
<td>61</td>
</tr>
<tr>
<td>Executive Committee</td>
<td>67</td>
</tr>
<tr>
<td>Technical Program Committee</td>
<td>68</td>
</tr>
<tr>
<td>Conference Sponsors</td>
<td>70</td>
</tr>
<tr>
<td>Hilton Hotel Map</td>
<td>73</td>
</tr>
</tbody>
</table>
GENERAL INFORMATION

Registration Hours & Location

**Location: Terrazza Foyer**

- **Monday, November 5**: 7:00am – 6:00pm
- **Tuesday, November 6**: 7:30am – 6:00pm
- **Wednesday, November 7**: 7:30am – 6:00pm
- **Thursday, November 8**: 7:00am – 4:00pm

**ICCAD 2018 Mobile App**

Review the program, save sessions to your personalized conference schedule, read speakers abstracts, and connect with other attendees using the ICCAD 2018 mobile app provided by Whova, available for download today. Download Whova and search for ICCAD 2018.

**Proceedings**

ICCAD Conference Papers will be delivered electronically online via a username and password. To access: http://proceedings.iccad.com

- **Badge ID** = Registration ID (on your badge)
- **Your Email** = Email address

Please refer to your registration receipt to access the files you are eligible to view.
GENERAL INFORMATION

Parking Information
Discounted event self-parking of $15.00 per vehicle per night.
Daytime rates $5.00 up to three hours; $8.00 for three - six hours; $12 for six - twelve hours.

For Speakers & Presenters

SPEAKERS’ BREAKFAST
Please attend the day of your presentation!

Location: Terrazza Ballroom
Monday, November 5 7:30 - 8:15am
Tuesday, November 6 7:30 - 8:15am
Wednesday, November 7 7:30 - 8:15am

NEED PRACTICE?
An AV Practice Room will be available in Private Dining Room (PDR), set up with a computer, LCD projector, and screen for you to practice/view your slides before your session.

Location:
Monday, November 5 7:00 - 9:30am and 3:00 - 6:00pm
Tuesday, November 6 7:00 - 9:30am
Wednesday, November 7 7:00 -11:00am and 4:00 - 6:00pm

ICCAD Social Media
Connect with ICCAD through Twitter @ICCAD. ICCAD will be tweeting hourly updates and conference highlights

Stay Connected during the Conference
ICCAD 2018 is offering internet access in the meeting rooms for attendees.
The Wi-Fi connection is Hilton Resort, user name: iccad2018 password: iccad2018.

Conference Management
Our mission is to facilitate networking, education and marketing with efficiency and precision in order to maximize customer experiences, and client profitability and recognition. We accomplish this by having a committed staff of trade show production organizers with the training, technology tools, processes and experience to offer the best service in the industry.
Visit mpassociates.com for more information.
In the spirit of the long-running ACM programming contest, the CADathlon is a challenging, all-day, programming competition focusing on practical problems at the forefront of Computer-Aided Design, and Electronic Design Automation in particular. The contest emphasizes the knowledge of algorithmic techniques for CAD applications, problem-solving and programming skills, as well as teamwork.

In its seventeenth year as the “Olympic games of EDA,” the contest brings together the best and the brightest of the next generation of CAD professionals. It gives academia and the industry a unique perspective on challenging problems and rising stars, and it also helps attract top graduate students to the EDA field.

The contest is open to two-person teams of graduate students specializing in CAD and currently full-time enrolled in a Ph.D granting institution in any country. Students are selected based on their academic backgrounds and their relevant EDA programming experiences. Travel grants are provided to qualifying students. The CADathlon competition consists of six problems in the following areas:

1. Circuit design and analysis
2. Physical design and design for manufacturability
3. Logic and high-level synthesis
4. System design and analysis
5. Verification and testing
6. Future technologies (Bio-EDA, Security, AI, etc.)

More specific information about the problems and relevant research papers will be released on the Internet one week prior to the competition. The writers and judges that construct and review the problems are experts in EDA from both academia and industry. At the contest, students will be given the problem statements and example test data, but they will not have the judges’ test data. Solutions will be judged on correctness and efficiency. Where appropriate, partial credit might be given. The team that earns the highest score is declared the winner. In addition to handsome trophies, the first and second place teams will receive cash award.

Contest winners will be announced at the ICCAD Opening Session on Monday morning and celebrated at the ACM/SIGDA Dinner and Member Meeting.

The CADathlon competition is sponsored by ACM/SIGDA and several Computer and EDA companies. For detailed contest information and sample problems from last year’s competition, please visit the ACM/SIGDA website at http://www.sigda.org/programs/cadathlon

For all inquiries, please send emails to: cadathlon@gmail.com

ORGANIZING COMMITTEE:
Chair, Iris Hui-Ru Jiang, National Taiwan University
Vice Chair, Tsung-Wei Huang, University of Illinois Urbana-Champaign
Vice Chair, Pei-Yu Lee, Muxeda Technology
NSF Workshop on Internet-of-Things (IoT) Systems
**Time: 8:30am - 5:30pm | Room: Portofino**

Organizer:
Marilyn Wolf - Georgia Institute of Technology

Internet-of-Things systems are widely used in disciplines including manufacturing, logistics, and medicine. As IoT systems increase in scope and complexity, new challenges are presented. The workshop will explore emerging challenges and identify research opportunities with the goal of improving the capabilities and use case repertoire of IoT technology. Workshop participants will create a report on research challenges in IoT systems.

Bias Buster Workshop @ ICCAD
**Time: 5:00 - 8:00pm | Room: Marseilles**

Speakers:

Gerry Katilius  
Google, Inc.

Diana Marculescu  
Carnegie Mellon Univ.

Unconscious (or implicit) bias is believed to be a significant factor that inhibits inclusivity and acts to stall or even thwart important efforts for increasing and celebrating diversity. Everyone has implicit or unconscious biases, and because they are unconscious, we are unaware of them. In this workshop, the first of its kind at ICCAD, the basis of implicit bias is presented and effective tools for increasing awareness and mitigation of its unwanted effects are provided. This important workshop is useful to every ICCAD participant—bystanders and advocates alike—who can intervene and effectively bust implicit bias when it occurs, either in themselves or in others. The workshop will present current understanding of what these biases are and how we can reduce their impacts in our behaviors and interactions with others. There will be role-playing activities to give attendees practice at identifying and responding to unconscious bias in day-to-day activities.

Background: Bias Busters @ Work (BB@Work) was created by Google as an extension of its Unconscious Bias @ Work Workshop (UB@Work), a course aimed at raising awareness of how unconscious biases work, how they can negatively influence workplace interactions, and what tools can help disrupt bias. In 2015, Google and Carnegie Mellon University created the Bias Busters @ University program, with Bias Busters@CMU being a version specifically tailored for Carnegie Mellon, first piloted by CMU’s College of Engineering and School of Computer Science. More information on Bias Busters @ Work: https://rework.withgoogle.com/subjects/unbiasing
IEEE/ACM William J. McCalla
ICCAD Best Paper Award Candidates

MONDAY, NOVEMBER 5

1A.2* Analytical Solution of Poisson’s Equation and Its Application to VLSI Global Placement
   Wenxing Zhu - Fuzhou Univ.
   Zhipeng Huang - Fuzhou Univ.
   Jianli Chen - Fuzhou Univ.
   Yao-Wen Chang - National Taiwan Univ.

TUESDAY, NOVEMBER 6

5C.1* DNNBuilder: an Automated Tool for Building High-Performance DNN Hardware Accelerators for FPGAs
   Xiaofan Zhang - Univ. of Illinois at Urbana-Champaign
   Junsong Wang - IBM Research - China
   Chao Zhu - IBM Research - China
   Yonghua Lin - IBM Research - China
   Jinjun Xiong - IBM T.J. Watson Research Center
   Wen-Mei Hwu - Univ. of Illinois at Urbana-Champaign
   Deming Chen - Univ. of Illinois at Urbana-Champaign

WEDNESDAY, NOVEMBER 7

8A.2* Parallelizable Bayesian Optimization for Analog and Mixed-Signal Rare Failure Detection with High Coverage
   Hanbin Hu - Texas A&M Univ.
   Peng Li - Texas A&M Univ.
   Jianhua Z. Huang - Texas A&M Univ.

9A.2* GPU Acceleration of RSA is Vulnerable to Side-channel Timing Attacks
   Chao Luo - Northeastern Univ.
   Yunsi Fei - Northeastern Univ.
   David Kaeli - Northeastern Univ.

9B.1* SODA: Stencil with Optimized Dataflow Architecture
   Yuze Chi - Univ. of California, Los Angeles
   Jason Cong - Univ. of California, Los Angeles
   Peng Wei - Univ. of California, Los Angeles
   Peipei Zhou - Univ. of California, Los Angeles

10B.1* PolyCleaner: Clean your Polynomials before Backward Rewriting to Verify Million-gate Multipliers
   Alireza Mahzoon - Universität Bremen
   Daniel Große - Universität Bremen / DFKI
   Rolf Drechsler - Universität Bremen / DFKI
IEEE/ACM William J. McCalla ICCAD Best Paper Award Selection Committee

Joerg Henkel (Chair) - Karlsruhe Institute of Technology
Yier Jin - Univ. of Florida
Youngsoo Shin - Korea Advanced Institute of Science and Technology
Wei Zhang - Hongkong Univ. of Science and Technology
Zheng Zhang - Univ. of California, Santa Barbra
Tulika Mitra - National Univ. of Singapore

Ten-Year Retrospective Most Influential Paper Award Selection Committee

Naehyuck Chang (Chair) - Korea Advanced Institute of Science and Technology
Ulf Schlichtmann - Tech. Univ. of Munich
Thomas Wenisch - Univ. of Michigan
Evangeline Young - Chinese Univ. of Hong Kong
Ramesh Karri - New York Univ.
Sung-Kyu Lim - Georgia Institute of Tech.

TUTORIAL/SPECIAL SESSION COMMITTEE

Yiran Chen - Duke University
Shao-Yun Fang - National Taiwan Univ.
Tim Güneysu - University of Bochum/DFKI
Diana Marculescu - Carnegie Mellow Univ.
Sherief Reda - Brown Univ.
Robert Wille - Univ. of Linz

WORKSHOP SELECTION COMMITTEE

Naehyuck Chang - Korea Advanced Institute of Science and Technology
Jörg Henkel - Karlsruhe Institute of Technology
MONDAY SCHEDULE

8:30 - 9:00am
Opening Session & Awards
Location: Saint Tropez

9:00 - 10:00am
Adventures and Opportunities in Cyber-Physical Systems Research
Chandra Krintz - Univ. of California, Santa Barbara | Location: Saint Tropez

10:00 - 10:30am
Coffee Break
Location: Terrazza Foyer

10:30am - 12:30pm
Session 1A: Analytical Techniques in Design Planning
Location: Saint Tropez

Session 1B: Ahoy! Anti-Piracy Techniques
Location: Monte Carlo

Session 1C: Flexibility Makes Learning Better
Location: Riveria

Special Session 1D: Emerging Reconfigurable Nanotechnologies: Can they Support Future Electronics?
Location: Capri

11:30am - 1:30pm
ACM Student Research Competition Poster Session
Location: Private Dining Room

12:45 - 1:45pm
Lunch
Location: Bayside Terrace
MONDAY SCHEDULE

1:45 - 3:45pm
Session 2A: It’s Time to Learn More About Timing, Power, and IR Drop!
Location: Saint Tropez

Embedded Tutorial 2B: Accelerated Safe and Secure Machine Learning
Location: Monte Carlo

Session 2C: Architecting for Efficiency of Deep Learning
Location: Riveria

Special Session 2D: EDA for Cyber-Physical Systems
Location: Capri

4:00 - 4:30pm
Coffee Break
Location: Terrazza Foyer

4:15 - 5:45pm
Session 3A: Generate, Stimulate and Simulate!
Location: Saint Tropez

Session 3B: Sweet Memories of Deep Learning
Location: Monte Carlo

Session 3C: Adaptive Power and Precision Optimization Using Machine Learning and Approximate Computing
Location: Riveria

Special Session 3D: 2018 CAD Contest at ICCAD
Location: Capri

5:45 - 6:15pm
A New Era in Digital Routing
Location: Saint Tropez

6:15 - 6:45pm
Networking Reception
Location: Frescos Lounge

6:45 - 8:15pm
ACM Student Research Competition Technical Presentations
Location: Saint Tropez
Opening Session and Awards

**Time: 8:30 - 10:00am | Location: Saint Tropez**

Kick off the conference with opening remarks from the ICCAD Executive Committee members and hear the highlights of the conference. The IEEE/ACM William J. McCalla ICCAD Best Paper award will be announced along with other award presentations from IEEE and ACM.

**IEEE/ACM WILLIAM J. MCCALLA ICCAD BEST PAPER AWARD**

This award is given in memory of William J. McCalla for his contributions to ICCAD and his CAD technical work throughout his career.

**Front-End Award:**

5C.1 **DNNBuilder: An Automated Tool for Building High-Performance DNN Hardware Accelerators for FPGAs**

- Xiaofan Zhang - Univ. of Illinois at Urbana-Champaign
- Junsong Wang - IBM Research - China
- Chao Zhu - IBM Research - China
- Yonghua Lin - IBM Research - China
- JinJun Xiong - IBM T.J. Watson Research Center
- Wen-Mei Hwu - Univ. of Illinois at Urbana-Champaign
- Deming Chen - Univ. of Illinois at Urbana-Champaign

**Back-End Award:**

10B.1 **PolyCleaner: Clean Your Polynomials Before Backward Rewriting to Verify Million-Gate Multipliers**

- Alireza Mahzoon - Universität Bremen
- Daniel Grosse - Universität Bremen / DFKI
- Rolf Drechsler - Universität Bremen / DFKI

**TEN YEAR RETROSPECTIVE MOST INFLUENTIAL PAPER AWARD**

This award is being given to the paper judged to be the most influential on research and industrial practice in computer-aided design over the ten years since its original appearance at ICCAD.

2008 Paper Titled: **A Low-Overhead Fault Tolerance Scheme for TSV-Based 3D Network on Chip Links**

- Igor Loi - University of Bologna
- Subhasish Mitra - Thomas H. Lee, Stanford University
- Shinobu Fujita - Toshiba
- Luca Benini - University of Bologna
- ICCAD 2008, pp. 598 - 602

**2018 ACM/SIGDA PIONEER AWARD**

Alberto L. Sangiovanni-Vincentelli, Edgar L. and Harold H. Buttrn Chair of Electrical Engineering and Computer Sciences at the University of California at Berkeley

For pioneering and fundamental contributions to design automation research and industry in system-level design, embedded systems, logic synthesis, physical design and circuit simulation.

**IEEE CEDA OUTSTANDING SERVICE RECOGNITION**

- Sri Parameswaran - University of New South Wales

For outstanding service to the EDA community as ICCAD General Chair in 2017.

**IEEE CEDA ERNEST S. KUH EARLY CAREER AWARD**

- Paul Bogdan - University of Southern California

For contributions to network-on-chip interconnects for multi-core cyber-physical systems.

**IEEE CAS TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS PRIZE PAPER AWARD**

Paper entitled "**Wireless NoC and Dynamic VFI Co-Design: Energy Efficiency without Performance Penalty**"

- Ryan Gary Kim, Wonje Choi, Zhuo Chen, Partha Pratim Pande, Diana Marculescu, and Radu Marculescu

**ACM/SIGDA CADATHALON**

Introduction of the 2018 winners.
Through the convergence of recent advances in device and control systems, sensor networks, data analytics, and cloud computing, Cyber-physical systems (CPS) is on course to transform our society and disrupt the way humans engineer and interact with the world around them. CPS tightly integrates communications and computation into ordinary physical objects and amalgamates them as systems, enabling them to collect vast amounts of data about their environment, to extract inferences and predictions from the data, and to use this information to automate, enhance, actuate, control, and optimize operations and decision making at a variety of scales. In this talk, we discuss some of the key technological advances that are spurring CPS innovation, we detail our experiences employing CPS to optimize agricultural processes as part of the UCSB SmartFarm project, and we describe the opportunities and challenges that are emerging in CPS research.

**Biography:** Chandra Krintz is Professor of Computer Science at UC Santa Barbara and Chief Scientist and Co-founder of AppScale Systems Inc. Chandra holds M.S./Ph.D. degrees in CS from UC San Diego. Her research interests lie at the cross-section of cloud computing and programming systems and her contributions improve performance, reduce energy consumption, and simplify the use of heterogeneous, distributed systems. Chandra has supervised and mentored over 60 students, published her work in a wide range of top venues, and participated in numerous outreach efforts to introduce computing to young people. Chandra’s efforts have been recognized with a NSF CAREER award, the CRA-W Anita Borg Early Career Award, and the UCSB Academic Senate Distinguished Teaching Award. She was also named a Cloud Computing Pioneer by Information Week and a top M2M Woman by Connected World.
MONDAY, NOVEMBER 5

Coffee Break
Time: 10:00 - 10:30am | Room: Terrazza Foyer

1A - Analytical Techniques in Design Planning
Time: 10:30am - 12:30pm | Room: Saint Tropez

Moderator:
Sabya Das - Synopsys, Inc.

The papers in this session propose techniques to address different challenges in the physical design flow. The first paper considers the thermal aspect of design during the floorplanning stage. The second paper proposes an analytical solution of Poisson’s equation to solve global placement, and the third one suggests proximal group ADMM approach for foggy and proximity effects-aware placement. Finally, the fourth paper discusses efficient partitioning and grouping for Timing-driven Multiplexing in FPGA designs.

1A.1 A Fast Thermal-Aware Fixed-Outline Floorplanning Methodology Based on Analytical Models
Jai-Ming Lin, Tai-Ting Chen, Yen-Fu Chang, Wei-Yi Chang - National Cheng Kung Univ.
Ya-Ting Shyu, Yeong-Jar Chang, Juin-Ming Lu - Industrial Technology Research Institute

1A.2* Analytical Solution of Poisson’s Equation and Its Application to VLSI Global Placement
Wenxing Zhu, Zhipeng Huang, Jianli Chen - Fuzhou Univ.
Yao-Wen Chang - National Taiwan Univ.

1A.3 Novel Proximal Group ADMM for Placement Considering Fogging and Proximity Effects
Jianli Chen, Li Yang, Zheng Peng, Wenxing Zhu - Fuzhou Univ.
Yao-Wen Chang - National Taiwan Univ.

1A.4 Simultaneous Partitioning and Signal Grouping for Time-Division Multiplexing in 2.5D FPGA-Based Systems
Shih-Chun Chen - National Taiwan Univ.
Richard Sun - Synopsys, Inc.
Yao-Wen Chang - National Taiwan Univ.

All speakers are denoted in bold | * denotes Best Paper Candidate
1B - Ahoy! Anti-Piracy Techniques

**Time: 10:30am - 12:30pm | Room: Monte Carlo**

Moderators:
- Tauhidur Rahman - Univ. of Alabama
- Ujjwal Guin - Auburn Univ.

Piracy attacks have been threatening the IC industry. This session explores the new territories of trusted manufacturing in reversible computing, 3D ICs, analog mixed-signal, and timing countermeasures. The first paper explains how reversible circuits can be used to prevent piracy and reverse engineering. The second paper proposes an attack on timing locks. The third one extends the boundary of logic locking to analog and mixed-signal systems, and the last paper solves split manufacturing and camouflaging problems in 3D systems.

**1B.1 IC/IP Piracy Assessment of Reversible Logic**

Samah Saeed - City Univ. of New York
Xiaotong Cui - Chongqing Univ.
Alwin Zulehner, Robert Wille - Johannes Kepler Univ. Linz
Rolf Drechsler - Universität Bremen
Kaijie Wu, Ramesh Karri - New York Univ.

**1B.2 TimingSAT: Timing Profile Embedded SAT Attack**

Abhishek Chakraborty, Yuntao Liu, Ankur Srivastava - Univ. of Maryland, College Park

**1B.3 Towards Provably-Secure Analog and Mixed-Signal Locking Against Overproduction**

Nithyashankari Gummidi, Jayasankaran, Adriana Sanabria Borbon, Edgar Sanchez-Sinencio, Jiang Hu, Jeyavijayan Rajendran - Texas A&M Univ.

**1B.4 Best of Both Worlds: Integration of Split Manufacturing and Camouflaging into a Security-Driven CAD Flow for 3D ICs**

Satwik Patnaik - New York Univ.
Mohammed Ashraf, Ozgur Sinanoglu, Johann Knechtel - New York Univ., Abu Dhabi

All speakers are denoted in bold | * denotes Best Paper Candidate
1C - Flexibility Makes Learning Better

*Time: 10:30am - 12:30pm | Room: Riveria*

**Moderator:**
Deming Chen - Univ. of Illinois at Urbana-Champaign

Efficient training and deployment of neural networks are critical. The first paper in this session discusses a novel quantization scheme using powers-of-arbitrary-log-bases, and the second paper presents a processing in-DRAM framework for binary CNNs. The third paper proposes AXNet, a neural network based approximate computing allowing holistic end-to-end training. The last paper in this session proposes a scalable-effort CNN (ConvNet) that allows effort-accuracy scalability for classification of data at multi-level abstraction.

1C.1 **Efficient Hardware Acceleration of CNNs Using Logarithmic Data Representation With Arbitrary Log-Base**
Sebastian Vogel - Robert Bosch GmbH
Mengyu Liang - Tech. Univ. of Munich
Andre Guntoro - Robert Bosch GmbH
Walter Stechele - Tech. Univ. of Munich
Gerd Ascheid - RWTH Aachen Univ.

1C.2 **NID: Processing Binary Convolutional Neural Network in Commodity DRAM**
Jaehyeong Sim, Hoseok Seol, Lee-Sup Kim - Korea Advanced Institute of Science and Technology

1C.3 **AXNet: ApproXimate Computing Using an End-to-End Trainable Neural Network**
Zhenghao Peng, Li Jiang, Xuyang Chen, Chengwen Xu, Naifeng Jing, Xiaoyao Liang, Cewu Lu - Shanghai Jiao Tong Univ.

1C.4 **Scalable-Effort ConvNets for Multilevel Classification**
Valentino Peluso, Andrea Calimera - Politecnico di Torino

All speakers are denoted in bold | * denotes Best Paper Candidate
Several emerging reconfigurable technologies have been explored in recent years offering device level runtime reconfigurability. These technologies offer the freedom to choose between p- and n-type functionality from a single transistor. In order to optimally utilize the feature-sets of these technologies, circuit designs and storage elements require novel design to complement the existing and future electronic requirements. An important aspect to sustain such endeavors is to supplement the existing design flow from the device level to the circuit level. This should be backed by a thorough evaluation so as to ascertain the feasibility of such explorations. Additionally, since these technologies offer runtime reconfigurability and often encapsulate more than one functions, hardware security features like camouflaging layouts and polymorphic logic gates come naturally cheap with circuits based on these reconfigurable technologies. This session presents innovative approaches to be devised for optimal circuit designs harnessing the reconfigurable features of these nanotechnologies. New circuit design paradigms based on these nano devices will be discussed to brainstorm on exciting avenues for novel computing elements.
Additional Meeting - ACM Student Research Competition Poster Session

**Time: 11:30am - 1:30pm | Room: Private Dining Room**

Sponsored by Microsoft Research, the ACM Student Research Competition (SRC) is an internationally recognized venue enabling undergraduate and graduate students who are members of ACM and ACM SIGDA to:

- Experience the research world—for many undergraduates this is a first!
- Share research results and exchange ideas with other students, judges, and conference attendees.
- Rub shoulders with academic and industry luminaries.
- Understand the practical applications of their research.
- Perfect their communication skills.
- Receive prizes and gain recognition from ACM, and the greater computing community.

ACM SRC has three rounds:

1. abstract review
2. poster session (this session)
3. technical presentation

In the first round, 2-page research abstracts are evaluated by EDA experts from academia and industry to select participants for the second round (this session). For the ACM SRC at ICCAD 2018 competition, 20 participants were selected to present their research at ICCAD.

The posters are evaluated by EDA experts to select up to 5 participants in graduate and undergraduate categories to advance to the final round (technical presentation round). Students are expected to discuss their work with judges. Each judge will rate the student’s visual presentation based on the criteria of uniqueness of the approach, the significance of the contribution, visual presentation, and quality of presentation.

More details can be found at: sigda.org/src

---

**Lunch**

**Time: 12:30 - 1:30pm | Room: Bayside Terrace**

Join fellow attendees for lunch in Terrazza Ballroom.
2A - It’s Time to Learn More About Timing, Power, and IR Drop!
*Time: 1:45 - 3:45pm | Room: Saint Tropez*

**Moderator:**
Chung-Kuan Cheng - Univ. of California, San Diego

This session covers the state of the art advances in timing, power, and IR drop analysis in both digital and analog design. Suitability in the end-to-end design methodology will be the feature focus, along with applications of machine learning to this challenging domain.

2A.1 **Design and Algorithm for Clock Gating and Flip-Flop Co-Optimization**
Giyoung Yang, Taewhan Kim - Seoul National Univ.

2A.2 **Macro-Aware Row-Style Power Delivery Network Design for Better Routability**
Jai-Ming Lin, Jhih-Sheng Syu, I-Ru Chen - National Cheng Kung Univ.

2A.3 **Modeling and Optimization of Magnetic Core TSV-Inductor for On-Chip DC-DC Converter**
Baixin Chen - Zhejiang Univ.
Umamaheswara Tida - Univ. of Notre Dame
*Cheng Zhuo* - Zhejiang Univ.
Yiyu Shi - Univ. of Notre Dame

2A.4 **Machine-Learning-Based Dynamic IR Drop Prediction for ECO**
Yen-Chun Fang, Heng-Yi Lin, **Min-Yan Su**, Chien-Mo Li - National Taiwan Univ.
Eric Jia-Wei Fang - MediaTek, Inc.
Embedded Tutorial 2B - Accelerated Safe and Secure Machine Learning

*Time: 1:45 - 3:45pm | Room: Monte Carlo*

This tutorial brings the top experts from the industry and academia to cover several important topics in safe, and secure machine learning that enable automated synthesis of trustworthy machine learning for the state-of-the-art algorithms. The discussed topics include ML on private (encrypted) data, model assurance against the contemporary attacks including adversarial learning and transfer learning, IP protection for ML, as well as trusted execution of contemporary ML algorithms. Due to its prevalence and dominance in state-of-the-art applications, deep learning would be utilized as the proof-of-concept for the various discussed methodologies.

The tutorial provides a unique opportunity for the audience to gain a thorough understanding of deep learning models, the security, privacy and reliability issues of the existing methodologies, and potential solutions to address the standing issues in the context of (deep) learning models. Emphasis will be given to safe and secure automation and acceleration of the explained methodologies using hardware-software co-design techniques. Given the wide range of ML applications in various scientific fields and the increasing interest of academia and industry leaders in this emerging field, this tutorial prepares the audience to attain a competitive advantage by providing a holistic view of the existing security and privacy concerns in automated systems empowered by ML and the state-of-the-art hardware-software co-design solutions to address those concerns.

2B.1 **Deep Learning on Encrypted Data**
Farinaz Koushanfar, M. Sadegh Riazi - Univ. of California, San Diego

2B.2 **Machine Learning IP Protection**
Rosario Cammarota - Qualcomm Technologies, Inc.

2B.3 **Assured Deep Learning: Practical Defense Against Adversarial Attacks**
Bita Rouhani - Microsoft Corporation
Mohammad Samragh, Mojan Javaheripi, Tara Javidi, Farinaz Koushanfar - Univ. of California, San Diego

2B.4 **Trusted Execution for Machine Learning**
Ahmad-Reza Sadeghi - Technische Univ. Darmstadt

All speakers are denoted in bold | * denotes Best Paper Candidate
2C - Architecting for Efficiency of Deep Learning

Time: 1:45 - 3:45pm | Room: Riveria

Moderator:
Meng Li - Facebook AI Silicon Research

The papers of this session aim to improve the efficiency of deep learning systems via optimizing the architecture for hardware, algorithm, and design methodology. The first two papers propose new hardware architecture for deep neural network accelerators. The third paper designs a new neural network architecture for energy-constrained applications. The fourth paper presents neural network-based design methodology for timing error prediction.

2C.1 Tetris: Re-Architecting Convolutional Neural Network Computation for Machine Learning Accelerators
Hang Lu, Xin Wei, Ning Lin, Guihai Yan, Xiaowei Li - Chinese Academy of Sciences

2C.2 FCN-Engine: Accelerating Deconvolutional Layers in Classic CNN Processors
Dawen Xu, Kaijie Tu - Hefei Univ. of Technology
Ying Wang - Chinese Academy of Sciences
Heng Liu, Bingsheng He - National Univ. of Singapore
Huawei Li - Chinese Academy of Sciences

2C.3 Designing Adaptive Neural Networks for Energy-Constrained Image Classification

2C.4 FATE: Fast and Accurate Timing Error Prediction Framework for Low Power DNN Accelerator Design
Jeff Zhang, Siddharth Garg - New York Univ.

All speakers are denoted in bold | * denotes Best Paper Candidate
Special Session 2D - EDA for Cyber-Physical Systems

**Time: 1:45 - 3:45pm | Room: Capri**

**Moderators:**
- Samarjit Chakraborty - Technical Univ. of Munich
- Mohammad Al Faruque - Univ. of California, Irvine

From automating tasks in the domain of integrated circuits design, Electronic Design Automation (EDA) has been moving up the design abstraction ladder, now encompassing many system-level design tasks. The next challenge facing the EDA community is to develop methods and also tools for cyber-physical systems (CPS) design. However, currently available EDA tools and methods cannot handle these complex CPSs where the physical processes, the control algorithms and the computation and communication platforms are all modeled and designed in a tightly integrated fashion. There exists a gap between the communities dealing with different aspects of CPS design and the goal of this special session is to address these challenges in order to effectively design and validate large-scale CPSs. In particular, it will feature talks on four important CPS application areas and discuss the need for EDA methods and tools in these areas.

### 2D.1 Waterfall is Too Slow, Let’s go Agile: Multi-Domain Coupling for Synthesizing Automotive Cyber-Physical Systems

Debayan Roy, Michael Balszun - Technical Univ. of Munich  
**Thomas Heurung** - Siemens Industry Software GmbH, Germany  
Samarjit Chakraborty - Technical Univ. of Munich  
Amol Naik - Siemens Corp.

### 2D.2 Model-Based and Data-Driven Approaches for Building Automation and Control

Tianshu Wei - Univ. of California, Riverside  
Xiaoming Chen - Chinese Academy of Sciences  
Xin Li - Duke Univ.  
Qi Zhu - Northwestern Univ.

### 2D.3 Future Automation Engineering Using Structural Graph Convolutional Neural Networks

Jiang Wan - Univ. of California, Irvine  
Blake S. Pollard - Carnegie Mellon Univ.  
Sujit Rokka Chhetri, Mohammad Abdullah Faruque - Univ. of California, Irvine  
**Arquimedes Canedo** - Siemens Corp.  
Palash Goyal - Univ. of Southern California

### 2D.4 Design Automation for Battery Systems

Swaminathan Narayanaswamy, Sangyoung Park, Sebastian Steinhorst,  
Samarjit Chakraborty - Technical Univ. of Munich

Coffee Break

**Time: 3:45pm - 4:15pm | Room: Terrazza Foyer**

All speakers are denoted in bold | * denotes Best Paper Candidate
3A - Generate, Stimulate and Simulate!

**Time: 4:15 - 5:45pm | Room: Saint Tropez**

**Moderator:**
Nagaraj Kelageri - Qualcomm Technologies, Inc.

Effective generation of stimuli is a critical step in the verification flow. The three papers in this session present advances in this field. The first paper is focused on coverage-directed testing in FPGA environments using the insights developed in software verification. The second paper speeds the generation of directed tests for shared-memory multi-processor verification. The third paper presents a method that facilitates rapid generation of multiple and diverse stimuli from complex constraints.

**3A.1 RFUZZ: Coverage-Directed Fuzz Testing of RTL on FPGAs**
Kevin Lauefer, Jack Koenig, Donggyu Kim, Jonathan Bachrach, Koushik Sen - Univ. of California, Berkeley

**3A.2 Steep Coverage-Ascent Directed Test Generation for Shared-Memory Verification of Multicore Chips**
Gabriel Andrade, Marleson Graf, Nicolas Pfeifer, Luiz Dos Santos - Federal Univ. of Santa Catarina

**3A.3 SMTSampler: Efficient Stimulus Generation from Complex SMT Constraints**
Rafael Dutra, Jonathan Bachrach, Koushik Sen - Univ. of California, Berkeley

3B - Sweet Memories of Deep Learning

**Time: 4:15 - 5:45pm | Room: Monte Carlo**

**Moderator:**
Yanzhi Wang - Northeastern Univ.

Who doesn't remember the basics of deep learning! But can you design systems for in-memory computing using FeFETs that reduce power consumption and ReRAM that moderates data migration? The first paper in this session investigates reliable ReRAM-based deep learning with single-bit cells. The second paper introduces a power-efficient FeFET-based in-memory computing architecture, whereas the third paper designs and implements a system for multitask (transfer) learning using GPUs and ReRAM. Even as you learn new things, important information should stay in your memory!

**3B.1 DL-RSIM: A Simulation Framework to Enable Reliable ReRAM-Based Accelerators for Deep Learning**
Meng-Yao Lin - National Taiwan Univ.
Hsiang-Yun Cheng - Academia Sinica
Wei-Ting Lin, Tzu-Hsien Yang, I-Ching Tseng, Chia-Lin Yang - National Taiwan Univ.
Han-Wen Hu, Hung-Shen Chang, Hsiang-Pang Li - Macronix International Co., Ltd.
Meng-Fan Chang - National Tsing Hua Univ.

**3B.2 A Ferroelectric FET Based Power-Efficient Architecture for Data-Intensive Computing**
Yun Long, Taesik Na, Prakshi Rastogi, Karthik Rao, Asif Islam Khan, Sudhakar Yalamanchili, Salbal Mukhopadhyay - Georgia Institute of Technology

**3B.3 EMAT: An Efficient Multi-Task Architecture for Transfer Learning Using ReRAM**
Fan Chen, Hai Li - Duke Univ.
3C - Adaptive Power and Precision Optimization Using Machine Learning and Approximate Computing

**Time: 4:15 - 5:45pm | Room: Riveria**

**Moderator:**
Elaheh Bozorgzadeh - Univ. of California, Irvine

This session includes three papers which propose adaptive algorithms to optimize the energy efficiency and fixed-point precision. The first paper presents a novel reinforcement learning approach to co-optimize the power delivery and consumption of multicore systems. The second paper considered power-hungry augmented reality applications on mobile devices and presents an automated technique to minimize energy consumption without degrading the quality. Finally, the last paper employs a Q-Learning algorithm to adaptively optimize the precision of stochastic gradient descent in deep neural network (DNN) training.

### 3C.1 Co-Manage Power Delivery and Consumption for Manycore Systems Using Reinforcement Learning

**Haoran Li,** Zhongyuan Tian, Rafael Kioji Vivas Maeda, Xuanqi Chen, Jun Feng, Jiang Xu
Rafael Kioji Vivas Maeda, Xuanqi Chen, Jun Feng, Jiang Xu - The Hong Kong University of Science and Technology

### 3C.2 Adaptive-Precision Framework for SGD Using Deep Q-Learning

**Wentai Zhang,** Hanxian Huang, Jiaxi Zhang, Ming Jiang, Guojie Luo - Peking Univ.

### 3C.3 Differentiated Handling of Physical Scenes and Virtual Objects for Mobile Augmented Reality

**Chih-Hsuan Yen,** Wei-Ming Chen - National Taiwan Univ.
Pi-Cheng Hsu - Academia Sinica
Tei-Wei Kuo - National Taiwan Univ.
Special Session 3D - 2018 CAD Contest at ICCAD

**Time: 4:15 - 5:45pm | Room: Capri**

The CAD Contest at ICCAD (https://iccad-contest.org/) is a challenging, multi-month, research and development competition, focusing on advanced, real-world problems in the field of Electronic Design Automation (EDA). Contestants can participate in one or more problems provided by EDA/IC industry. The prizes will be awarded at an ICCAD special session dedicated to this contest.

Since 2012, the CAD Contest at ICCAD has been attracting more than a hundred teams per year (112 teams from 12 regions in 2015, 135 teams from 11 regions in 2016, and 123 teams from 10 regions in 2017), fostering productive industry-academia collaborations, and leading to hundreds of publications in top-tier conferences and journals. The contest keeps enhancing its impact and boosts EDA research.

3D.1 **Overview of 2018 CAD Contest at ICCAD**  
Mark Po-Hung Lin - National Chung Cheng Univ.

3D.2 **A: Smart EC: Program-Building for Name Mapping**  
Chi-An (Rocky) Wu - Cadence Design Systems, Inc.

3D.3 **Problem B: Obstacle-Aware On-Track Bus Routing**  
About Liao - Synopsys, Inc.

3D.4 **Problem C: Timing-Aware Fill Insertion**  
Bo Yang - Synopsys, Inc.

3D.5 **Paper Title: DATC RDF: An Academic Flow From Logic Synthesis to Detailed Routing**  
Jinwook Jung - Korea Advanced Institute of Science and Technology  
Iris Hui-Ru Jiang - National Taiwan Univ.  
Jianli Chen - Fuzhou Univ.  
Shih-Ting Lin, Yih-Lang Li - National Chiao Tung Univ.  
Victor Kravets, Gi-Joon Nam - IBM Research

Sponsored by:

All speakers are denoted in bold | * denotes Best Paper Candidate
Additional Meeting - A New Era in Digital Routing  
**Time:** 5:45 - 6:15pm | **Room:** Saint Tropez

**Speaker:**  
Wen-Hao Liu - Cadence Design Systems, Inc.

Routing problem becomes more and more complicated for the advanced technology nodes. If the design flow is not fully aware of routability, the design most likely cannot be fabricated at the end of the flow due to routability issues. This talk will introduce the modern routing challenges faced by digital design practitioners in the industry, and the speaker will share his experience about how to improve routability awareness for digital design tools from logical syntheses to detailed routing.

**Biography:** Wen-Hao Liu, received his Ph.D. degree in Computer Science from National Chiao Tung University, Taiwan in 2013. His research interests include routing, placement, and clock synthesis. Wen-Hao has published more than 30 papers and 5 patents in these fields, and he has served on the technical program committee of DAC, ICCAD, ISPD, and ASPDAC. Currently, Wen-Hao works at Cadence as a software architect. He is the main developer of the next-generation routing engines used in multiple Cadence’s tools, and he has involved in the technology node enablement for 16nm, 10nm, 7nm, 5nm, and 3nm.

Networking Reception  
**Time:** 6:15 - 6:45pm | **Room:** Frescos Lounge

Whatever your goal, networking receptions are the perfect venue for you to expand your network and keep you connected! Join us today to catch up with your colleagues and discuss the day’s presentations with the conference presenters. All attendees are invited.

Additional Meeting - ACM Student Research Competition Technical Presentations  
**Time:** 6:45 - 8:15pm | **Room:** Saint Tropez

The ACM Student Research Competition allows both graduate and undergraduate students to discuss their research with student peers, as well as academic and industry researchers, in an informal setting, while enabling them to attend ICCAD.

This session is the final round of ACM SRC at ICCAD 2018. Each student will present for 10 minutes, followed by a 2-minute question and answer period. This session will be attended by the evaluators and any interested conference attendees. The top three winners in each category will be chosen based on these presentations. The undergraduate and graduate finalists will be eligible to compete in the ACM SRC Grand Finals to be held in June 2019.

More details can be found at: sigda.org/src
Monday, November 5

TUESDAY SCHEDULE

8:30 - 10:00am
Session 4A: Device Optimization for Reliability and Performance Enhancement
  Location: Saint Tropez
Session 4B: Clean Up Your Data
  Location: Monte Carlo
Special Session 4C: Security of Emerging Architectures
  Location: Riveria
Special Session 4D: Machine Learning for Electronic Design Automation: Modeling, Optimization, and Resilience
  Location: Capri

10:00 - 10:30am
Coffee Break
  Location: Capri

10:30am - 12:00pm
Session 5A: The Non-Unified Theory of Approximate Computing
  Location: Saint Tropez
Session 5B: Resistance is Not Futile (for RAM)
  Location: Monte Carlo
Session 5C: High-Performance Deep Learning Accelerators on FPGAs
  Location: Riveria
Special Session 5D: Hardware Intellectual Property (IP) Protection Techniques: What, When, and How to Use?
  Location: Capri
Special Session 5E: Managing Heterogeneous Many-Cores for High-Performance and Energy-Efficiency
  Location: Private Dining Room

12:00 - 12:30pm
Lunch
  Location: Terrazza Ballroom

12:30 - 1:30pm
CEDA Invited Keynote: Analyzing the Disruptive Impact of a Silicon Compiler
  Andreas Olofsson - Defense Advanced Research Projects Agency
  Location: Terrazza Ballroom

All speakers are denoted in bold | * denotes Best Paper Candidate
TUESDAY SCHEDULE

1:45 - 3:45pm
Session 6A: Deep Dive into Mixed Size Cell Placement
   Location: Saint Tropez
Session 6B: Post-CMOS Technologies and Emerging Applications
   Location: Monte Carlo
Session 6C: Biochips, Blockchain, and Learning in CPS
   Location: Riveria
   Location: Capri
Embedded Tutorial 6E: Majority Logic Synthesis
   Location: Private Dining Room

3:45 - 4:15pm
Coffee Break
   Location: Terrazza Foyer

4:15 - 6:15pm
Session 7A: Routing: The Devil is in the Details
   Location: Saint Tropez
Session 7B: Synthesizing Neural, Parallel, and Approximate Logic
   Location: Monte Carlo
Session 7C: Build a Fort: Designing and Assessing Secure Architectures
   Location: Riveria
Special Session 7D: Security for Next-Generation Connected and Autonomous Vehicles
   Location: Capri
Embedded Tutorial 7E: The Need and Opportunities of Electromigration-Aware Integrated Circuit Design
   Location: Private Dining Room

6:15 - 6:45pm
Networking Reception
   Location: Frescos Lounge

6:45 - 8:30pm
ACM/SIGDA Member Meeting
   Location: Terrazza Ballroom
4A - Device Optimization for Reliability and Performance Enhancement

**Time: 8:30 - 10:00am | Room: Saint Tropez**

**Moderator:**
Takashi Sato - Kyoto Univ.

This session presents enhanced modeling and analysis to improve performance in a variety of devices while accounting for the effects of noise and aging induced delay increases. The first paper presents a novel analytical model of static noise margin in SRAM cells. The second paper enhances the reliability of circuits by handling transistor aging through adaptive voltage guardbanding with online monitoring. The last paper presents models for analyzing the variation of transistor characteristics in flexible electronics, and proposes practical methods for its compensation.

**4A.1 Physical Modeling of Bitcell Stability in Subthreshold SRAMs for Leakage-Area Optimization Under PVT Variations**
Xin Fan - RWTH Aachen Univ.
Rui Wang - Intrinsic ID
Tobias Gemmeke - RWTH Aachen Univ.

**4A.2 Comparing Voltage Adaptation Performance Between Replica and In-Situ Timing Monitors**
Yutaka Masuda - Osaka Univ.
Jun Nagayama, Hirotaka Takeno, Yoshimasa Ogawa, Yoichi Momiyama - Socionext, Inc.
Masanori Hashimoto - Osaka Univ.

**4A.3 Strain-Aware Performance Evaluation and Correction for OTFT-Based Flexible Displays**
Tengtao Li, Sachin S. Sapatnekar - Univ. of Minnesota

4B - Clean Up Your Data

**Time: 8:30 - 10:00am | Room: Monte Carlo**

**Moderator:**
Tulika Mitra - National Univ. of Singapore

This session focuses on managing data in a secure and energy-efficient manner for SSD storage and bus-based communication architectures. The papers in this session propose novel strategies for fast sanitization of data in MLC Flash memory, secure data placement in SSDs, and energy-efficient approximations when sending data over on-chip buses.

**4B.1 Achieving Fast Sanitization with Zero Live Data Copy for MLC Flash Memory**
Ping-Hsien Lin - Macronix International Co., Ltd.
Yu-Ming Chang - National Taiwan Univ.
Yung-Chun Li, Wei-Chen Wang - Macronix International Co., Ltd.
Chien-Chung Ho - National Chung Cheng Univ.
Yuan-Hao Chang - Academia Sinica

**4B.2 Architecting Data Placement in SSDs for Efficient Secure Deletion Implementation**
Hoda Aghaei Khouzani - Univ. of Delaware
Chen Liu - Intel Corp.
Chengmo Yang - Univ. of Delaware

**4B.3 AxBA: An Approximate Bus Architecture Framework**
Jacob R. Stevens, Ashish Ranjan, Anand Raghunathan - Purdue Univ.
Special Session 4C - Security of Emerging Architectures

**Time: 8:30 - 10:00am | Room: Riveria**

**Moderator:**
Farinaz Koushanfar - Univ. of California, San Diego

Computing of tomorrow will critically rely on radically new architectural paradigms, driven by a new set of applications, including deep learning, real-time classification of massive arrays of sensor data, comprehension and pattern recognition in big-data sets. Emerging architectures offer tremendous advantages with respect to various design objectives, but one important target has been neglected so far: security. Adversarial attacks can target a system’s communication links, the software running on it, and the humans using it. However, the system’s hardware is increasingly considered its Achilles’ heel, as more and more attacks targeting the physical implementation of security-relevant functions. Recent purely hardware-oriented attacks called Meltdown and Spectre compromised millions of installed systems. The proposed session will consider the intricate relationship between emerging architectures and security from two sides. The first two talks will focus on security implications of novel architectural concepts: approximate computing and neuromorphic multi-processor SoCs. These paradigms are currently discussed without considering security, although systems designed according to these principles are well-suitable for security-critical tasks, like area surveillance or intrusion detection. The third talk will take a different approach: How should highly complex heterogeneous systems be designed when security is taken into account from the beginning? Security solutions discussed in the session will have to be addressed by holistic strategies where CAD tools will play a main role.

**4C.1 Security: The Dark Side of Approximate Computing?**
Francesco Regazzoni, Cesare Alippi - Univ. of Lugano
Ilia Polian - Univ. of Stuttgart

**4C.2 Security Aspects of Neuromorphic MPSoCs**
Johanna Sepulveda - Technical Univ. of Munich
Cezar Reinbrecht - Delft Univ. of Technology
Jean-Philippe Diguet - Centre National de la Recherche Scientifique

**4C.3 Vulnerability-Tolerant Secure Architectures**
Todd Austin, Valeria Bertacco, Baris Kasikci - Univ. of Michigan
Sharad Malik - Princeton Univ.
Mohit Tiwari - Univ. of Texas at Austin
Special Session 4D - Machine Learning for Electronic Design Automation: Modeling, Optimization, and Resilience

*Time: 8:30 - 10:00am | Room: Capri*

**Moderator:**
Pande Partha - Washington State University

The rate of growth of Big Data, slowing down of Moore’s law, and the rise of emerging applications pose significant challenges in the design of large-scale computing systems with high-performance, energy-efficiency, and reliability. This special session will consider solutions based on machine learning and data analytics to address the following challenges: (1) How can we model the performance and power consumption of heterogeneous systems and interconnects using machine learning techniques? (2) How to use machine learning and statistical modeling for effective design space exploration of computing systems to optimize for power, performance, and thermal metrics? (3) How to use machine learning techniques to efficiently manage resources of computing systems (e.g., power, memory, interconnects) to improve performance and energy-efficiency? (4) How can data analytics facilitate fault diagnosis, detect anomalies, and increase robustness in the network backbone of emerging large-scale networking systems? To address these outstanding challenges, out-of-the-box approaches need to be explored. By integrating machine learning algorithms, data analytics, statistical modeling, and design of advanced computing systems, this session will engage a broad section of ICCAD conference attendees. This special session is targeted towards university researchers/professors, students, industry professionals, and computing system designers. This session will attract newcomers who want to learn how to apply machine learning and data analytics to solve problems in computing systems, as well as experienced researchers looking for exciting new directions in computing systems design, EDA methodologies, and multi-scale computing. This special session covers design, optimization and resilience: three main pillars of designing computing systems. It also highlights how machine learning and EDA researchers can join hands to design energy-efficient and reliable chips and systems.

**4D.1 Machine Learning for Performance and Power Modeling of Heterogeneous Systems**
Joseph Greathouse, Gabriel Loh - Advanced Micro Devices, Inc.

**4D.2 Machine Learning for Design Space Exploration and Optimization of Manycore Systems**
Ryan Gary Kim - Colorado State Univ.
Janardhan Rao Doppa, Partha Pratim Pande - Washington State Univ.

**4D.3 Failure Prediction Based on Anomaly Detection for Complex Core Routers**
Shi Jin - Duke Univ.
Zhaobo Zhang - Huawei Technologies Co., Ltd.
Krishnendu Chakrabarty - Duke Univ.
Xinli Gu - Huawei Technologies Co., Ltd.

Coffee Break

*Time: 10:00am - 10:30am | Room: Terrazza Foyer*

Sponsored by: Huawei

All speakers are denoted in bold | * denotes Best Paper Candidate
5A - The Non-Unified Theory of Approximate Computing

Time: 10:30am - 12:00pm | Room: Saint Tropez

Moderator:
Nektarios Tsoutsos - Univ. of Delaware.

This session deals with trading off computational accuracy and energy efficiency. The first paper explores a novel classifier-approximator architecture for approximate computing on a low-power accelerator. The second paper advocates a new approach based on stochastic computing to trade off accuracy and circuit level efficiency. The final paper advocates a theoretically-robust methodology for optimizing multi-output approximate logic.

5A.1 Invocation-Driven Neural Approximate Computing with a Multiclass-Classifier and Multiple Approximators
Haiyue Song, Li Jiang, Chengwen Xu, Zhuoran Song, Naifeng Jing,
Xiaoyao Liang - Shanghai Jiao Tong Univ.
Qiang Xu - The Chinese University of Hong Kong

5A.2 Deterministic Methods for Stochastic Computing Using Low-Discrepancy Sequences
M. Hassan Najafi, David Lilja, Marc Riedel - Univ. of Minnesota

5A.3 Design Space Exploration of Multi-Output Logic Function Approximations
Jorge Echavarria, Stefan Wildermann,
Jürgen Teich - Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU)

5B - Resistance is Not Futile (for RAM)

Time: 10:30am - 12:00pm | Room: Monte Carlo

Moderator:
Chengmo Yang - Univ. of Delaware

Resistive RAM (ReRAM) is an emerging non-volatile storage and near-memory computing solution that promises to disrupt traditional computing as we know it. The papers in this session propose a robust hybrid ReRAM fabric, explore the use of energy-efficient and fast logic implementations in ReRAM fabrics, and the use of ReRAM in executing emerging deep learning workloads.

5B.1 3DICT: A Reliable and QoS Capable Mobile Process-In-Memory Architecture for Lookup-Based CNNs in 3D XPoint ReRAMs
Qian Lou - Indiana University Bloomington
Wujie Wen - Florida International Univ.
Lei Jiang - Indiana University Bloomington

5B.2 Aliens: A Novel Hybrid Architecture for Resistive Random-Access Memory
Bing Wu, Dan Feng, Wei Tong, Jingning Liu, Shuai Li, Mingshun Yang, Chengning Wang,
Yang Zhang - Huazhong University of science and technology

5B.3 FELIX: Fast and Energy-Efficient Logic in Memory
Saransh Gupta - Univ. of California, San Diego
Mohsen Imani - University of California San Diego
Tajana Rosing - Univ. of California, San Diego

All speakers are denoted in bold | * denotes Best Paper Candidate
5C - High-Performance Deep Learning Accelerators on FPGAs

**Time: 10:30am - 12:00pm | Room: Riveria**

**Moderator:**
Yingyan Lin - Rice Univ.

For both edge-devices and cloud servers, FPGA accelerators for deep neural networks have delivered favorable reconfigurability and performance. However, long hardware design time, prior homogeneous designs, and irregularities in deep learning algorithms have limited the achievable throughput and latency. To address these, the papers in this session present automated RTL generation with fine-grained pipelining, hardware-optimized algorithm adaptation, and integration of heterogeneous accelerators.

**5C.1**

**DNNBuilder: An Automated Tool for Building High-Performance DNN Hardware Accelerators for FPGAs**
Xiaofan Zhang - Univ. of Illinois at Urbana-Champaign
Junsong Wang, Chao Zhu, Yonghua Lin - IBM Research - China
Jinjun Xiong - IBM T.J. Watson Research Center
Wen-Mei Hwu, Deming Chen - Univ. of Illinois at Urbana-Champaign

**5C.2**

**Algorithm-Hardware Co-Design of Single Shot Detector for Fast Object Detection on FPGAs**
Yufei Ma - Arizona State Univ.
Tu Zheng - Fuzhou Univ.
Yu Cao, Sarma Vrudhula, Jae-Sun Seo - Arizona State Univ.

**5C.3**

**TGPA: Tile-Grained Pipeline Architecture for Low Latency CNN Inference**
Xuechao Wei, Yun (Eric) Liang - Peking Univ.
Xiuhong Li - Peking University, Beijing
Cody Hao Yu - Univ. of California, Los Angeles
Peng Zhang - Falcon Computing Solutions, Inc.
Jason Cong - Univ. of California, Los Angeles
Special Session 5D - Hardware Intellectual Property (IP) Protection Techniques: What, When, and How to Use?

Time: 10:30am - 12:00pm | Room: Capri

Moderator:
Ozgur Sinanoglu - New York Univ., Abu Dhabi

Globalization of Integrated Circuit (IC) design is forcing the IC/IP designers and users re-assess their trust in hardware. As the IC design flow spans the globe, driven by cost-conscious consumer electronics, hardware is increasingly prone to new kinds of attacks such as counterfeiting, hardware Trojans, side channel analysis, reverse engineering and IP piracy. An attacker, anywhere within this design flow, can reverse engineer the functionality of an IC/IP, steal and claim ownership of the IP, inject malicious circuitry (i.e., hardware Trojans) into the IC, or introduce counterfeits into the supply chain. Moreover, an untrusted IC fab may overbuild ICs and sell them illegally. The semiconductor industry is estimated to lose $4 billion annually due to these attacks.

Many of these attacks hinge on the fact the attacker can obtain full control over the design. To thwart such adversaries, researchers have developed several techniques, namely IP metering, logic locking/encryption, camouflaging, and split manufacturing. These techniques are currently being used and/or considered for usage by companies. These techniques greatly differ in their threat models and security properties. Together, they address a wide spectrum of attackers—untrusted designer, untrusted foundry, untrusted testing facility, untrusted user, and a combination thereof.

This tutorial brings in three experts on these topics to explain these techniques in a collective and cohesive way. The tutorial will explain what techniques to use against attackers, when to use them in the supply-chain, and how to use them in a provably-secure way. Techniques will be explained using concepts from IC design and test, graph theory, and cryptography. The presenters collectively have more than two decades of research experience in these topics, providing a wide coverage from theory to practice.

5D.1 IP Protection in Untrusted Supply Chain
Farinaz Koushanfar - Univ. of California, San Diego

5D.2 Customized Locking of IP Blocks on a Multi-Million-Gate SoC
Ozgur Sinanoglu - New York Univ., Abu Dhabi
Abhrajit Sengupta - New York Univ.
Mohammed Nabeel, Mohammed Ashraf - New York Univ., Abu Dhabi

5D.3 Split Manufacturing
Jeyavijayan Rajendran - Texas A&M Univ.
Special Session 5E - Managing Heterogeneous Many-Cores for High-Performance and Energy-Efficiency

**Time:** 10:30am - 12:00pm | **Room:** Private Dining Room

**Moderator:**
- Siddharth Garg - New York Univ.

Heterogeneity has become the Swiss army knife for designing energy-efficient and thermally safe systems ranging from simple edge devices to high-performance multi-core processing platforms. Integration of application-specific heterogeneous accelerators and general-purpose cores deliver programmable systems-on-chip (SoCs) with superior performance and significantly lower power footprint compared to homogenous architectures. This special session presents the state-of-the-art in form of three talks covering Resource Management, Online learning and Communication Architectures for heterogeneous Many-Cores.

**5E.1 Dynamic Resource Management for Heterogeneous Many-Cores**
- Jörg Henkel - Karlsruhe Institute of Technology
- Jürgen Teich, Stefan Wildermann - Friedrich-Alexander-Universität Erlangen-Nürnberg
- Hussam Amrouch - Karlsruhe Institute of Technology

**5E.2 Online Learning for Adaptive Optimization of Heterogeneous SoCs**
- Ganapati Bhat, Sumit Mandal, Umit Ogras - Arizona State Univ.
- Ujjwal Gupta - Intel Corp.

**5E.3 Hybrid On-Chip Communication Architectures for Heterogeneous Manycore Systems**
- Biresh Kumar Joardar, Janardhan Rao Doppa, Partha Pratim Pande - Washington State Univ.
- Diana Marculescu, Radu Marculescu - Carnegie Mellon Univ.

**Lunch**

**Time:** 12:00 - 1:30pm | **Room:** Terrazza Ballroom

Join fellow attendees for lunch in Terrazza Ballroom.
CEDA Invited Luncheon Talk - Analyzing the Disruptive Impact of a Silicon Compiler

*Time: 12:30 - 1:30pm | Room: Terrazza Ballroom*

**Speaker:**

**Andreas Olofsson** - Defense Advanced Research Projects Agency

Recent years have seen an explosion in the cost and time required to design advanced System-on-Chips (SoCs), systems-in-packages (SiPs), and PCBs. As part of the $1.5B Electronics Resurgence Initiative (ERI), DARPA is building the world’s first general purpose silicon compilers. The effort involves two distinct research programs, the Intelligent Design of Electronic Assets (IDEA) program aiming to create a no-human-in-the-loop layout generator for digital and analog circuits, and the Posh Open Source Hardware (POSH) program aiming to create a high quality trustable open source ecosystem. Together the efforts will create a universal hardware compiler capable of automatically generating production ready GDSII drawings directly from rich catalog of trustable source code and schematics for digital as well as analog circuits. Achieving this ambitious goal will require advancing the state of the art in machine learning, optimization algorithms, expert systems, and verification technology. This talk will discuss technical challenges associated with building a universal hardware compiler and provide analysis of potential economic and societal impacts.

**Biography:** Mr. Andreas Olofsson joined DARPA as a program manager in the Microsystems Technology Office in January 2017. His interests include intelligent design automation, system optimization, and open hardware. Prior to his arrival at DARPA, Mr. Olofsson devoted 20 years to designing and testing low-power processors and mixed-signal circuits at Texas Instruments, Analog Devices, and Adapteva. Chip products designed by Mr. Olofsson include low-power digital signal processors (DSPs), charge-coupled device (CCD) readout circuits, and massively parallel reduced instruction set computing (RISC) processors. From 2008 to 2016, Mr. Olofsson served as the CEO of Adapteva, where he developed the Epiphany architecture and Parallellela open source computer. The Parallellela democratized access to parallel computing and catalyzed the growth of a community of 10,000 developers and 200 universities across the globe. Mr. Olofsson received his Bachelor of Science in Physics and Electrical Engineering and Master of Science in Electrical Engineering from the University of Pennsylvania. Mr. Olofsson is a member of IEEE and holds nine U.S. patents.
6A - Deep Dive into Mixed Size Cell Placement

**Time: 1:45 - 3:45pm | Room: Saint Tropez**

**Moderator:**
Ismail Bustany - Xilinx Inc.

In the physical design placement implementation flow, mixed-height cells introduce additional challenges, such as Poly-alignment, fence regions, multi-cell spacing, and technology constraints. In this session, the first paper addresses the challenges involving the multi-cell spacing constraint. The remaining three papers address the problems related to technology and fence region constraints.

6A.1 **A Practical Detailed Placement Algorithm under Multi-Cell Spacing Constraints**
Yu-Hsiang Cheng, Ding-Wei Huang, Wai-Kei Mak, Ting-Chi Wang - National Tsing Hua Univ.

6A.2 **Mixed-Cell-Height Placement Considering Drain-to-Drain Abutment**
Yu-Wei Tseng, Yao-Wen Chang - National Taiwan Univ.

6A.3 **Mixed-Cell-Height Legalization Considering Technology and Region Constraints**
Ziran Zhu, Xingquan Li, Yuhang Chen, Jianli Chen, Wenxing Zhu - Fuzhou Univ.
Yao-Wen Chang - National Taiwan Univ.

6A.4 **Mixed-Cell-Height Placement with Complex Minimum-Implant-Area Constraints**
Jianli Chen, Peng Yang, Xingquan Li, Wenxing Zhu - Fuzhou Univ.
Yao-Wen Chang - National Taiwan Univ.

6B - Post-CMOS Technologies and Emerging Applications

**Time: 1:45pm - 3:45pm | Room: Monte Carlo**

**Moderator:**
Deliang Fan - Univ. of Central Florida

This session covers the post-CMOS technologies and the related emerging applications. The resistive memory (memristor) device is proposed as the enabling technology for main memory, routing switch in FPGA, and synaptic weight in neural network accelerators. An Ising processor with approximated parallel tempering is proposed to improve the quality of optimization solutions.

6B.1 **RAPID: Read Acceleration for Improved Performance and Endurance in MLC/TLC NVMs**
Poovaiah Manavattira Palangappa, Kartik Mohanram - Univ. of Pittsburgh

6B.2 **Sneak Path Free Reconfiguration of Via-Switch Crossbars Based FPGA**
Ryutaro Doi, Jaehoon Yu, Masanori Hashimoto - Osaka Univ.

6B.3 **Mixed Size Crossbar based RRAM CNN Accelerator with Overlapped Mapping Method**
Zhenhua Zhu, Jilin Lin - Tsinghua Univ.
Ming Cheng - EE departement of tsinghua university
Lixue Xia, Hanbo Sun - Tsinghua Univ.
Xiaoming Chen - Chinese Academy of Sciences
Yu Wang, Huazhong Yang - Tsinghua Univ.

6B.4 **Enhancing the Solution Quality of Hardware Ising-Model Solver via Parallel Tempering**
Hideonori Gyoten, Masayuki Hiromoto, Takashi Sato - Kyoto Univ.

All speakers are denoted in bold | * denotes Best Paper Candidate
6C - Biochips, Blockchain, and Learning in CPS

**Time: 1:45 - 3:45pm | Room: Riveria**

**Moderators:**
- Umit Ogras - Arizona State Univ.
- Mohammad Al Faruque - Univ. of California, Irvine

Cyber-Physical Systems serve as the fabric of modern and future intelligent world. The first two papers of the session cover Artificial Neural Networks as enabler for CPS, one on the hardening of deep neural networks against adversarial attacks, and the other on reinforcement learning for wearable devices. The third and fourth papers are on two emerging applications of CPS, biochips and blockchain.

6C.1* **Defensive Dropout for Hardening Deep Neural Networks Under Adversarial Attacks**
- Siyue Wang - Northeastern Univ.
- Xiao Wang - Boston Univ.
- Pu Zhao - Northeastern Univ.
- Wujie Wen - Florida International Univ.
- David Kaeli - Northeastern Univ.
- Peter Chin - Boston Univ.
- Xue Lin - Northeastern Univ.

6C.2 **Online Human Activity Recognition Using Low-Power Wearable Devices**
- Ganapati Bhat, Ranadeep Deb, Vatika Vardhan Chaurasia - Arizona State Univ.
- Holly Shill - Barrow Neurological Institute
- Umit Y. Ogras - Arizona State Univ.

6C.3 **Shadow Attacks on MEDA Biochips**
- Mohammed Shayan - New York Univ.
- Sukanta Bhattacharjee - New York Univ., Abu Dhabi
- Tung-Che Liang - Duke Univ.
- Jack Tang - New York Univ.
- Krishnendu Chakrabarty - Duke Univ.
- Ramesh Karri - NYU

6C.4 **LeapChain: Efficient Blockchain Verification for Embedded IoT**
- Emanuel Regnath - Tech. Univ. of Munich
- Sebastian Steinhorst - Technical Univ. of Munich, Nanyang Technological Univ.

**Time: 1:45 - 3:45pm | Room: Capri**

**Moderators:**
- Houman Homayoun - George Mason Univ.
- Sam Gu - FutureWei Technologies, Inc.

In the recent years, Machine Learning (ML) especially mammalian brain inspired neural networks (including deep neural networks (DNNs)) have demonstrated an impressive performance and robustness to noise in different domains ranging from medical imaging, autonomous driving to defense applications. Despite DNNs being robust to noise and perturbations, recent research works have exploited the vulnerabilities and showed that the DNNs can be fooled by adding specially crafted perturbations to the input. In this session, first talk will introduce the challenges of ML in adversarial settings. This will be followed by two talks on making the ML inference robust to adversarial attacks in robotics and security domains. The last talk will provide an analysis of different adversarial attacks and solutions to improve the efficiency of existing defense techniques.

**6D.1 Robust Object Estimation using Generative-Discriminative Inference for Secure Robotics Applications**
Zhefan Ye, Odest Chadwicke Jenkins, Shiyang Lu, Zhiqiang Sui - Univ. of Michigan
R. Iris Bahar, Alessandro Costantini, Yanqi Liu - Brown Univ.

**6D.2 Adversarial Evasion Resilient Hardware Malware Detectors**
Dmitry Ponomarev - Binghamton Univ.
Khaled Khasawneh - Univ. of California, Riverside
Lei Yu - Binghamton Univ.
Nael Abu-Ghazaleh - Univ. of California, Riverside

**6D.3 Efficient Utilization of Adversarial Training towards Robust Machine Learners and its Analysis**
Sai Manoj, Sairaj Amberkar, Setareh Rafatirad, Houman Homayoun - George Mason Univ.
Embedded Tutorial 6E - Majority Logic Synthesis

**Time: 1:45 - 3:45pm | Room: Private Dining Room**

**Moderator:**
Mathias Soeken - École Polytechnique Fédérale de Lausanne

The majority function evaluates to true, if at least two of its Boolean inputs evaluate to true. The majority function has frequently been studied as a central primitive in logic synthesis applications for many decades. Knuth refers to the majority function in the last volume of his seminal The Art of Computer Programming as “probably the most important ternary operation in the entire universe.”

Majority logic synthesis has recently regained significant interest in the design automation community due to nanoemerging technologies which operate based on the majority function. In addition, majority logic synthesis has successfully been employed in CMOS-based applications such as standard cell or FPGA mapping. The tutorial gives a broad introduction into the field of majority logic synthesis. It will review fundamental results and describe recent contributions from theory, practice, and applications.

6E.1 **Practical Majority Logic Synthesis**
Luca Amarù - Synopsys, Inc.

6E.2 **Decomposing n-ary Majority Functions**
Eleonora Testa, Mathias Soeken,
Winston Haaswijk - École Polytechnique Fédérale de Lausanne
Luca Amarù - Synopsys, Inc.
Giovanni De Micheli - École Polytechnique Fédérale de Lausanne

6E.3 **Efficient Normal Form Systems for Representing Boolean Functions**
Miguel Couceiro - Univ. of Lorraine
Erkko Lehtonen - Technische Univ. Dresden
Pierre Mercuriali, - Univ. of Lorraine
Abdallah Saffidine - Australian National University

6E.4 **Overview of Emerging Non-Charge-Based Majority Logic Technologies**
Odysseas Zografos - IMEC

6E.5 **Majority Logic Synthesis**
Luca Amarù - Synopsys, Inc.
Eleonora Testa - École Polytechnique Fédérale de Lausanne
Miguel Couceiro - Univ. of Lorraine
Odysseas Zografos - IMEC
Giovanni De Micheli - École Polytechnique Fédérale de Lausanne
Mathias Soeken - École Polytechnique Fédérale de Lausanne

**Coffee Break**

**Time: 3:45 - 4:15pm | Room: Terrazza Foyer**

Sponsored by: HUAWEI

All speakers are denoted in bold | * denotes Best Paper Candidate
7A - Routing: The Devil is in the Details

**Time: 4:15 - 6:15pm | Room: Saint Tropez**

**Moderator:**
Gracieli Posser - Cadence Design Systems, Inc.

Continuous technology node shrinking and the increased complicated design rules have made detailed routing one of the most contentious parts of the physical design. In this session, the first paper discusses machine learning based routing congestion and violation prediction methods. This is followed by two papers on initial detailed routing. The session concludes with a paper on an open net locator for ECO routing.

7A.1 **RouteNet: Routability Prediction for Mixed-Size Designs Using Convolutional Neural Network**
Zhiyao Xie - Duke Univ.
Yu-Hung Huang, Guan-Qi Fang - National Taiwan Univ. of Science and Technology
Haoxing Ren - NVIDIA Corp.
Shao-Yun Fang - National Taiwan Univ. of Science and Technology
Yiran Chen - Duke Univ.
Jiang Hu - Texas A&M Univ.

7A.2 **[Anonymous]: An Initial Detailed Router for Advanced VLSI Technologies**
Andrew Kahng, Lutong Wang, Bangqi Xu - Univ. of California, San Diego

7A.3 **A Multithreaded Initial Detailed Routing Algorithm Considering Global Routing Guides**
Fan-Keng Sun, Hao Chen, Chen-Hao Hsu, Ching-Yu Chen, Yao-Wen Chang - National Taiwan Univ.

7A.4 **Extending ML-OARSMT to Net Open Locator with Efficient and Effective Boolean Operations**
Bing-Hui Jiang, Hung-Ming Chen - National Chiao Tung Univ.
7B - Synthesizing Neural, Parallel, and Approximate Logic

**Time: 4:15 - 6:15pm | Room: Monte Carlo**

**Moderator:**
Paras Gupta - Qualcomm Technologies, Inc.

The emergence of machine learning and artificial intelligence presents new challenges to hardware design and synthesis. In this session, the first two papers present the synthesis of logic originated from neural networks: with binary weights or threshold logic. The third paper discusses the use of approximate computing in logic optimization with delay-driven approximate synthesis framework. The last paper demonstrates how to accelerate logic synthesis with AIG rewriting.

7B.1* **Logic Synthesis of Binarized Neural Networks for Efficient Circuit Implementation**  
Chia-Chih Chi, Jie-Hong Roland Jiang - National Taiwan Univ.

7B.2 **Canonicalization of Threshold Logic Representation and Its Applications**  
Siang-Yun Lee, Nian-Ze Lee, Jie-Hong Roland Jiang - National Taiwan Univ.

7B.3 **DALS: Delay-Driven Approximate Logic Synthesis**  
Zhuangzhuang Zhou, Yue Yao, Shuyang Huang, Sanbao Su, Chang Meng, Weikang Qian - Shanghai Jiao Tong Univ.

7B.4 **Unlocking Fine-Grain Parallelism for AIG Rewriting**  
Vinicius Possani - Federal University of Rio Grande do Sul  
Yi-Shan Lu - Univ. of Texas at Austin  
Alan Mishchenko - Univ. of California, Berkeley  
Keshav Pingali - Univ. of Texas at Austin  
Renato Ribas, André Reis - Federal University of Rio Grande do Sul

7C - Build a Fort: Designing and Assessing Secure Architectures

**Time: 4:15 - 6:15pm | Room: Riveria**

**Moderator:**
Nektarios Tsoutsos - Univ. of Delaware

Fixing the security bugs post-deployment is impractical. This section explores novel solutions in assessing the security of a design and building secure architectures, which can be leveraged during design time. The first paper strengthens high-level synthesis tools to verify security properties. The second paper speeds up hardware security verification. The third paper builds a trusted architecture for heterogeneous systems. The final paper utilizes split manufacturing to thwart Trojans.

7C.1 **High-Level Synthesis With Timing-Sensitive Information Flow Enforcement**  

7C.2 **Property Specific Information Flow Analysis for Hardware Security Verification**  
Wei Hu - Northwestern Polytechnical Univ.  
Armaiti Ardestiricham, Mustafa Gobulukoglu - University of California San Diego  
Xinmu Wang - Northwestern Polytechnical Univ.  
Ryan Kastner - Univ. of California, San Diego

7C.3 **HISA: Hardware Isolation-Based Secure Architecture for CPU-FPGA Embedded Systems**  
Mengmei Ye, Xianglong Feng, Sheng Wei - University of Nebraska-Lincoln

7C.4 **SWAN: Mitigating Hardware Trojans With Design Ambiguity**  
Timothy Linscott, Valeria Bertacco, Todd Austin - Univ. of Michigan

All speakers are denoted in bold | * denotes Best Paper Candidate
Special Session 7D - Security for Next-Generation Connected and Autonomous Vehicles

**Time: 4:15 - 6:15pm | Room: Capri**

**Modерators:**
- Qi Zhu - Northwestern Univ.
- Yier Jin - Univ. of Florida

Next-generation vehicles will perform autonomous and semi-autonomous functions via multi-modal sensing, real-time computation with machine learning techniques, in-vehicle communication using new bus protocols, and control of mechanical components. They will also commutate with other surrounding vehicles and infrastructures via vehicular ad-hoc networks (VANETs) to further improve vehicle safety and transportation efficiency. However, the emerging of autonomous driving and vehicular communication techniques provides malicious attackers with a variety of local and remote, cyber and physical attack surfaces. Recent studies have shown that security is becoming a pressing and challenging concern for next-generation vehicles. In this session, the four talks will introduce the security challenges for both single autonomous vehicles and vehicular networks, and present state-of-the-art solutions from hardware to software, and to network and system layers.

**7D.1  Security for Safety: A Path Toward Building Trusted Autonomous Vehicles**
Raj Gautam Dutta - Univ. of Central Florida
Yaodan Hu, Yier Jin - Univ. of Florida
Feng Yu, Teng Zhang - Univ. of Central Florida

**7D.2  Hardware-Accelerated Data Acquisition and Authentication for High-speed Video Streams on Future Heterogeneous Automotive Processing Platforms**
Martin Geier, Fabian Franzen, Samarjit Chakraborty - Tech. Univ. of Munich

**7D.3  Network and System Level Security in Connected Vehicle Applications**
Hengyi Liang, Matthew Jagielski - Northeastern Univ.
Bowen Zheng - Univ. of California, Riverside
Chung-Wei Lin - National Taiwan Univ.
Eunsuk Kang, Shinichi Shiraishi - Toyota InfoTechnology Center
Cristina Nita-Rotaru - Northeastern Univ.
Qi Zhu - Northwestern Univ.

**7D.4  A Safety and Security Architecture for Reducing Accidents in Intelligent Transportation Systems**
Qian Chen, Azizeh Sowan, Shouhuai Xu - Univ. of Texas at San Antonio

All speakers are denoted in bold | * denotes Best Paper Candidate
Embedded Tutorial 7E - The Need and Opportunities of Electromigration-Aware Integrated Circuit Design

**Time: 4:15 - 6:15pm | Room: Private Dining Room**

**Moderator:**
Jens Lienig - Technische Univ. Dresden

Electromigration (EM) is becoming a progressively intractable design challenge due to increased interconnect current densities. It has changed from something designers “should” think about to something they “must” think about, i.e. become a requirement. The International Roadmap for Devices and Systems (IRDS) and the International Technology Roadmap for Semiconductors (ITRS) predict that semiconductor scale and interconnect cross-sections in semiconductor technologies will decrease further over the coming years. This continuing trend of IC down-scaling can easily lead to current densities that exceed their maximum allowable values. While analog designers have been aware of this problem for some time, increasingly digital designs are also affected. Accordingly, the ITRS indicates that all of today’s minimum-sized interconnects are EM-affected. The trend towards smaller line widths and smaller cross-sectional areas will continue at least until 2027, accompanied by an alarming increase in current densities in ICs going forward. As a consequence of these dramatic developments, any up-to date physical design methodology must be EM-aware; how to achieve this is the subject of this tutorial.

We first introduce the physical electromigration process and present its specific characteristics that can be affected during VLSI physical design. Examples of EM countermeasures that are applied in today’s commercial design flows are presented next. Here, we show how to improve the EM robustness of metallization patterns, we also consider mission profiles to obtain application-oriented current-density limits. The third presentation investigates the increasing interaction of EM with thermal migration. Finally, we conclude with a discussion of application examples to shift from a traditional (post-layout) EM verification towards a pro-active EM-aware physical design process. These methodologies, such as an EM-aware routing, increase EM-robustness of the layout with the overall goal of reducing the negative impact of EM on the circuit’s reliability.

**7E.1 Motivation and Fundamentals of EM and its Mitigation in Today's Design Flows**
Jens Lienig - Technische Univ. Dresden

**7E.2 EM-Aware Layout Design and Mission Profiles in Industrial Practice**
Juergen Scheible - Robert Bosch Center for Power Electronics
Goeran Jerke - Robert Bosch GmbH

**7E.3 Interaction of Thermal Effects, Thermal Migration and Electromigration**
Roland Jancke - Fraunhofer Institute for Integrated Circuits

**7E.4 Methodologies for EM-Aware Design in Future Technology Nodes**
Steve Bigalke - Technische Univ. Dresden

**7E.5 Paper Title: The Need and Opportunities of Electromigration-Aware Integrated Circuit Design**
Steve Bigalke, Jens Lienig - Technische Univ. Dresden
Goeran Jerke - Robert Bosch GmbH
Juergen Scheible - Robert Bosch Center for Power Electronics
Roland Jancke - Fraunhofer Institute for Integrated Circuits

All speakers are denoted in bold | * denotes Best Paper Candidate
Networking Reception

**Time: 6:15 - 6:45pm | Room: Frescos Lounge**

Whatever your goal, networking receptions are the perfect venue for you to expand your network and keep you connected! Join us today to catch up with your colleagues and discuss the day’s presentations with the conference presenters. All attendees are invited.

Sponsored by: Synopsys

---

**Additional Meeting - ACM SIGDA Member Meeting**

**Time: 6:45 - 8:30pm | Room: Terrazza Ballroom**

The annual ACM/SIGDA Member Meeting will be held on Tuesday evening from 6:45 -8pm. The meeting is open for ACM SIGDA members to attend. Members of the Electronic Design Automation community who would like to learn more about SIGDA or get involved with SIGDA activities are also invited. Dinner and beverages will be served.

The meeting will begin with a brief overview of SIGDA, including its organization, activities, volunteering opportunities, and member benefits. We will then introduce this year’s SIGDA Pioneering Achievement award recipient with an informal presentation of their achievements. Next, the Outstanding Young Faculty Award winner will present a brief talk on his work. Finally, we will end the evening with the announcement of the winners of ACM Design Automation Student Research Competition taking place at this year’s ICCAD. We hope to see you there!

Sponsored by: ACM SIGDA
8:30 - 9:30am
Keynote: The Future is What You Make It: EDA in the Post-Moore Age
Rob Aitken - Arm, Ltd.
Location: Saint Tropez

9:30 - 10:00am
Coffee Break
Location: Terrazza Foyer

10:00am - 12:00pm
Session 8A: Computationally Efficient and Uncertainty Aware Analog and Mixed-Signal CAD
Location: Saint Tropez
Session 8B: When Design Space Exploration Meets with Modern Applications and Systems
Location: Monte Carlo
Session 8C: Enabling Embedded Learning, Security, and Predictability
Location: Riveria
Special Session 8D: Superconducting Electronics Design Automation (S-EDA): Recent Developments and Upcoming Challenges
Location: Capri

12:00 - 1:00pm
Lunch
Location: Bayside Terrace

1:15 - 3:15pm
Session 9A: Plug the Leaks: Side-Channel Attacks and Countermeasures
Location: Saint Tropez
Session 9B: High-Throughput Computing and Efficient Data Movement
Location: Monte Carlo
Session 9C: Advances in Neural Networks and Microfluidics
Location: Riveria
Special Session 9D: A Journey from Physics to System Level on the Reliability Tracks
Location: Capri
3:15 - 3:35pm
Coffee Break
  Location: Terrazza Foyer

3:45 - 5:15pm
Special Session 10A: Computer-Aided Design for Quantum Computation
  Location: Saint Tropez
Session 10B: Taming the Wild: Scalable Methods in Verification
  Location: Monte Carlo
Session 10C: Capturing Perturbation for DNN Security
  Location: Riveria
Special Session 10D: A Hardware Outlook on Machine Learning Applications
  Location: Capri

5:15 - 5:45pm
Networking Reception
  Location: Frescos Lounge
The Future is What You Make It: EDA in the Post-Moore Age

Time: 8:30 - 9:30am | Room: Saint Tropez

Speaker:

Rob Aitken - Arm, Ltd.

Electronic design, design automation and technology have always been linked, but as time progresses and layers of abstraction develop holes or outright crumble, the connections between them necessarily become tighter. It’s not enough to ask how future technology will shape EDA, we also need to ask how EDA will shape technology. The EDA tools of the future will need to deal with heterogenous systems that span more than a single die. They will also need to cover abstractions from device through application software. In addition, the slowing of Moore’s law will lead to increased pressure on both design and design tools to provide product differentiation. Long term trends towards new devices, compute models, and memory elements also play a role. This talk explores these trends and their implications, and offers suggestions about where we can be certain and where we face unknown.

Biography: Rob Aitken is an ARM Fellow and technology lead for ARM Research. He is responsible for technology direction of ARM research, including identifying disruptive technologies, monitoring the global technology landscape, and coordinating research efforts within and outside of ARM. His role includes developing strategic relationships with universities, consortia, and other key participants in the global research community. His research interests include emerging technologies, memory design, design for variability, resilient computing, and statistical design. He has published over 80 technical papers, on a wide range of topics including impacts of technology scaling, statistics of memory bit cell variability and the use of static current monitoring as a circuit testing and diagnostic mechanism. He holds 30 US patents. Dr. Aitken joined ARM as part of its acquisition of Artisan Components in 2004. Prior to Artisan, he worked at Agilent and HP. He has given keynote addresses, tutorials and short courses at conferences and universities worldwide. He holds a Ph.D. from McGill University in Canada. Dr. Aitken is an IEEE Fellow, and serves on a number of conference and workshop committees.
Coffee Break

*Time: 9:30 - 10:00am | Room: Terrazza Foyer*

8A - Computationally Efficient and Uncertainty Aware Analog and Mixed-Signal CAD

*Time: 10:00am - 12:00pm | Room: Saint Tropez*

**Moderators:**
- Chung-Kuan Cheng - Univ. of California, San Diego
- Zheng Zhang - Univ. of California, Santa Barbara
- Eli Chiprout - Intel Corp.

This session covers novel algorithms and design trends of analog/RF/mixed-signal circuits and systems. The first two papers discuss uncertainty qualification theory and machine learning techniques to significantly decrease computational complexity through sample reduction. The next paper addresses the numerical stability in transient circuit simulation. The final paper optimizes the topology of an optical network on chip.

8A.1 Uncertainty Quantification of Electronic and Photonic ICs with Non-Gaussian Correlated Process Variations
Chunfeng Cui, Zheng Zhang - Univ. of California, Santa Barbara

8A.2* Parallelizable Bayesian Optimization for Analog and Mixed-Signal Rare Failure Detection with High Coverage
Hanbin Hu, Peng Li, Jianhua Z. Huang - Texas A&M Univ.

8A.3 Transient Circuit Simulation for Differential Algebraic Systems Using Matrix Exponential
Pengwen Chen - National Chung Hsing Univ.
Chung-Kuan Cheng, Dongwon Park, Xinyuan Wang - Univ. of California, San Diego

8A.4 CustomTopo: A Topology Generation Method for Application-Specific Wavelength-Routed Optical NoCs
Mengchu Li, Tsun-Ming Tseng - Technische Univ. München
Davide Bertozzi, Mahdi Tala - University of Ferrara
Ulf Schlichtmann - Technische Univ. München

All speakers are denoted in bold | * denotes Best Paper Candidate
8B - When Design Space Exploration Meets with Modern Applications and Systems

*Time: 10:00am - 12:00pm | Room: Monte Carlo*

**Moderator:**
Jishen Zhao - Univ. of California, San Diego

This session explores the design space of application-specific systems in the format of networks-for-chiplet, networks-on-chip, and FPGAs. The first two papers focus on networks, one optimizes the network design in 2.5D systems across logical, physical, and circuit layers, while the other explores the design space of application-specific NoCs with Monte Carlo Tree Search and Markov models. The last two papers center on FPGAs. One presents a high-level-synthesis approach for maximizing performance of FPGA-based designs in the presence of dynamic loop bounds, while the other leverages machine learning to estimate FPGA performance and power without any analytical model.

**8B.1 A Cross-Layer Methodology for Design and Optimization of Networks in 2.5D Systems**
Ayse Coskun, Furkan Eris, Ajay Joshi - Boston Univ.
Andrew Kahng - Univ. of California, San Diego
Yenai Ma - Boston Univ.
Vaishnav Srinivas - Univ. of California, San Diego

**8B.2 Wavefront-MCTS: Multi-Objective Design Space Exploration of NoC Architectures Based on Monte Carlo Tree Search**
Yong Hu, Daniel Mueller-Gritschneder - Technical Univ. of Munich, Nanyang Technological Univ.
Ulf Schlichtmann - Tech. Univ. of Munich

**8B.3 HLS-Based Optimization and Design Space Exploration for Applications with Variable Loop Bounds**
Young-kyu Choi, Jason Cong - Univ. of California, Los Angeles

**8B.4 HLSPredict: Cross Platform Performance Prediction for FPGA High-Level Synthesis**
Kenneth O’Neal - University of California Riverside Computer Science
Mitch Liu - University of California Riverside
Hans Tang, Amin Kalantar, Kennen DeRenard, Philip Brisk - Univ. of California, Riverside

All speakers are denoted in bold | * denotes Best Paper Candidate
8C - Enabling Embedded Learning, Security, and Predictability

**Time: 10:00am - 12:00pm | Room: Riveria**

**Moderators:**
- Gabriel Rutsch - Infineon Technologies

This session is on self-contained code generation for enabling embedded deep learning, on hardware-assisted attestation for preventing control-flow and data-flow attacks, on side-channel attack detection, and on software randomization for improving timing analysis of stringent industrial systems.

**8C.1 C-GOOD: C-Code Generation Framework for Optimized On-Device Deep Learning**
Duseok Kang, Euiseok Kim, Inpyo Bae, Bernhard Egger, Soonhoi Ha - Seoul National Univ.

**8C.2 LiteHAX: Lightweight Hardware-Assisted Attestation of Program Execution**
Ghada Dessouky, Tigist Abera - Technische Universitaet Darmstadt
Ahmad Ibrahim - Technische Univ. Darmstadt
Ahmad-Reza Sadeghi - Technische Universitaet Darmstadt

**8C.3 SCADET: A Side-Channel Attack Detection Tool for Tracking Prime+Probe**
Majid Sabbagh, Yunsi Fei - Northeastern Univ.
Thomas Wahl - Northeastern University, Boston
A. Adam Ding - Northeastern Univ.

**8C.4 Industrial Experiences with Resource Management Under Software Randomization in ARINC653 Avionics Environments**
Leonidas Kosmidis - Barcelona Supercomputing Center
Cristian Maxim, Victor Jegu - Airbus S.A.S.
Francis Vatrinet - SYSGO
Francisco Cazorla - Barcelona Supercomputing Center

All speakers are denoted in bold | * denotes Best Paper Candidate
Special Session 8D - Superconducting Electronics Design Automation (S-EDA): Recent Developments and Upcoming Challenges

**Time: 10:00am - 12:00pm | Room: Capri**

**Moderator:**
Tsung-Yi Ho - National Tsing Hua Univ.

The special session offers attendees an opportunity to bridge the semiconductor ICs/system technology with the superconducting electronics and quantum computing technologies. The special session will first describe the most ambitious development program for superconducting electronics circuit design tools to date—the Intelligence Advanced Research Projects Activity (IARPA) SuperTools Program—and provide a comprehensive overview of the state of design tool development as well as the circuit technology in the superconducting electronics community. Earlier design software roadmaps and tools were focused heavily on the device and gate level, with reasonably simple synthesis at the level of thousands of gates. Superconducting electronics circuit design tools today are still fragmented, incomplete, and insufficient for the design of very large scale integration circuits. EDA tools should enable design and verification of integrated circuits from process modeling right up to full system yield and reliability modeling. Recent development and upcoming challenges of EDA tools for superconducting electronics will be discussed. The session will consist of four talks on complementary aspects of these emerging technologies, including technology overview, circuit technology, manufacturing, test, and physical design optimization. We believe that the special session will generate interest in this topic, leading to more research, future challenges, and several open problems in this area. This is a novel and multidisciplinary topic of relevance to the EDA community.

**8D.1 Single Flux Quantum Circuit Technology and CAD Overview**
Coenrad J. Fourie - Stellenbosch Univ. & Stellenbosch Univ.

**8D.2 Evolving Superconductor Circuit Technology**
Akira Fujimaki, Masamitsu Tanaka - Nagoya Univ.

**8D.3 Design Automation Methodology and Tools for Superconductive Electronics**
Massoud Pedram - Univ. of Southern California
Yanzhi Wang - Northwestern Univ.

**8D.4 Multi-Terminal Routing with Length-Matching for Rapid Single Flux Quantum Circuits**
Pei-Yi Cheng - National Tsing Hua Univ.
Kazuyoshi Takagi - Kyoto Univ.
Tsung-Yi Ho - National Tsing Hua Univ.
Lunch

**Time: 12:00 - 1:00pm | Room: Bayside Terrace**

Join fellow attendees for lunch in Terrazza Ballroom.

**9A - Plug the Leaks: Side-Channel Attacks and Countermeasures**

**Time: 1:15 - 3:15pm | Room: Saint Tropez**

**Moderator:**

Alric Althoff - Leidos

After twenty years, side-channel attacks are moving to new horizons. In this session, we have papers presenting attacks on GPUs, at board-level, on the elliptic-curve library, and active countermeasures against EM attacks. The first paper proposes an active defense against electromagnetic side-channel attacks by adjusting the power grid impedance. It includes both formal and EM simulation-based validation of the proposed defense. The second paper focuses on the challenges of mounting timing-based side-channel attacks on GPU accelerators and demonstrates a practical attack breaking the RSA. The third paper shows how to extend power based side-channel attacks from one FPGA to another co-located on the same board. The final paper of the session shows a novel attack on an open-source crypto library that includes conventional mitigation against side-channel attacks.

**9A.1 Electromagnetic Equalizer: An Active Countermeasure Against EM Side-Channel Attack**

Chenguang Wang, Yici Cai, Haoyi Wang, Qiang Zhou - Tsinghua Univ.

**9A.2* GPU Acceleration of RSA is Vulnerable to Side-Channel Timing Attacks**

Chao Luo, Yunsi Fei, David Kaeli - Northeastern Univ.

**9A.3 Remote Inter-Chip Power Analysis Side-Channel Attacks at Board-Level**

Falk Schellenberg - Ruhr Univ. Bochum

Dennis Gnad - Karlsruhe Institute of Technology

Amir Moradi - Ruhr Univ. Bochum

Mehdi Tahoori - Karlsruhe Institute of Technology

**9A.4 Effective Simple-Power Analysis Attacks of Elliptic Curve Cryptography on Embedded Systems**

Chao Luo, Yunsi Fei, David Kaeli - Northeastern Univ.
9B - High-Throughput Computing and Efficient Data Movement

**Time: 1:15 - 3:15pm | Room: Monte Carlo**

**Moderator:**
Jing Xie - Qualcomm Research

The papers in this session exploit code generation and transformation techniques to achieve high throughput and efficient data movement. The first paper presents a framework for efficiently mapping stencil computations to FPGA platforms while the second presents a compilation framework based on the polyhedral model that translates high-level arithmetic-intensive kernels to systolic arrays on FPGAs. The third paper extracts data access patterns from an application to partition memory and generate data reuse logic. The fourth paper proposes compiler-automated transformations to optimize data layout for streaming accesses in addition to parameter tuning methods for high performance and low energy.

**9B.1** *
**SODA: Stencil with Optimized Dataflow Architecture**  
Yuze Chi, Jason Cong, Peng Wei, Peipei Zhou - Univ. of California, Los Angeles

**9B.2**  
**PolySA: Polyhedral-Based Systolic Array Auto-Compilation**  
Jason Cong, Jie Wang - Univ. of California, Los Angeles

**9B.3**  
**An Efficient Data Reuse Strategy for Multi-Pattern Data Access**  
Wensong Li, Fan Yang, Hengliang Zhu, Xuan Zeng, Dian Zhou - Fudan Univ.

**9B.4**  
**Optimizing Data Layout and System Configuration on FPGA-Based Heterogeneous Platforms**  
Hou-jen Ko, Zhiyuan Li, Samuel Midkiff - Purdue Univ.
9C - Advances in Neural Networks and Microfluidics

**Time: 1:15 - 3:15pm | Room: Riveria**

**Moderators:**
- Francesco Regazzoni - Univ. of Lugano
- Ilia Polian - Univ. Stuttgart

Biology and biologically-inspired computing models are at the forefront of today and tomorrow’s economy. The first two papers in this session explore the hardware implementations of neural network models targeting applications ranging from prosthetics to speech recognition and computer vision. The third paper explores binarization as a way to reduce the cost and complexity of convolutional neural networks implemented in hardware. The last paper reports on a technique to reduce the number of valves required to control programmable microfluidic biochips, which will miniaturize and automate biochemical reactions for applications such as next-generation diagnostic tests.

### 9C.1 Design and Optimization of Edge Computing Distributed Neural Processor for Biomedical Rehabilitation with Sensor Fusion

Kofi Otseidu, Tianyu Jia, Joshua Byrne - Northwestern Univ.
Levi Hargrove - AbilityLab
Jie Gu - Northwestern Univ.

### 9C.2 Area-Efficient and Low-Power Face-to-Face-Bonded 3D Liquid State Machine Design

Bon Woong Ku - Georgia Institute of Technology
Yu Liu, Yingyezhe Jin, Peng Li - Texas A&M Univ.
Sung Kyu Lim - Georgia Institute of Technology

### 9C.3 DIMA: A Depthwise CNN In-Memory Accelerator

Shaahin Angizi, Zhezhi He, Deliang Fan - Univ. of Central Florida

### 9C.4 Multi-Channel and Fault-Tolerant Control Multiplexing for Flow-Based Microfluidic Biochips

Ying Zhu, Bing Li - Technical Univ. of Munich, Nanyang Technological Univ.
Tsung-Yi Ho - National Tsing Hua Univ.
Qin Wang, Hailong Yao - Tsinghua Univ.
Robert Wille - Johannes Kepler Univ. Linz
Ulf Schlachtmann - Technical Univ. of Munich, Nanyang Technological Univ.
Special Session 9D - A Journey from Physics to System Level on the Reliability Tracks

**Time: 1:15 - 3:15pm | Room: Capri**

**Moderators:**
- Sheldon Tan - Univ. of California, Riverside
- Hidetoshi Onodera - Kyoto Univ.
- Hussam Amrouch - Karlsruhe Institute of Technology

Reliability has become a significant challenge for design of current nanometer integrated circuits (ICs). Reliability degradation caused by aging effects (time-dependent degradations) and transient soft-errors (time-independent degradations) are becoming limiting constraints in emerging computing and communication platforms due to increased failure rates from the continuous transistor scaling, increasing process variations and aggressive power reductions. Reliability problems will get worse as future chips will show signs of aging much faster than the previous generations. To mitigate the increasing reliability and resiliency problems, holistic cross-layer solutions starting from physics and extending across circuit and architecture all the way up to system level are desired. This session consists of four presentations ranging from physics-based electromigration (EM) modeling analysis, Bias Temperature Instability (BTI)-aware timing analysis and optimization, random telegraph noise (RTN) modeling and characterization to soft-error verification via multi-level process simulation. The presentations will cover the most important VLSI reliability effects such as EM for interconnects and BTI, RTN for devices and system-level soft-errors and will address the intersection of physics, circuit and systems for reliability and resiliency modeling, design and optimization.

**9D.1 Multi-Physics-based FEM Analysis for Post-voiding Analysis of Electromigration Failure Effects**
Hengyang Zhao, Sheldon Tan - Univ. of California, Riverside

**9D.2 Estimating and Optimizing BTI Aging Effects: From Physics to CAD**
Hussam Amrouch, Victor Van Santen, Jörg Henkel - Karlsruhe Institute of Technology

A.K.M. Mahfuzul Islam - Univ. of Tokyo
Hidetoshi Onodera - Kyoto Univ.

**9D.4 Performance and Accuracy in Soft-Error Resilience Evaluation using the Multi-Level Processor Simulator ETISS-ML**
Daniel Müller-Gritschneder, Uzair Sharif, Ulf Schlichtmann - Tech. Univ. of Munich

---

Coffee Break

**Time: 3:15 - 3:45pm | Room: Terrazza Foyer**
Special Session 10A - Computer-Aided Design for Quantum Computation

**Time:** 3:45 - 5:15pm | **Room:** Saint Tropez

**Moderator:**
Robert Wille - Johannes Kepler Univ. Linz

Quantum computation is currently moving from an academic idea to a practical reality. The recent past has seen tremendous progress in the physical implementation of corresponding “quantum computers” – also involving “big players” such as Google, IBM, Intel, Rigetti, Microsoft, and Alibaba. The corresponding devices promise substantial speedups over conventional computers for applications like quantum chemistry, optimization, machine learning, cryptography, quantum simulation, or systems of linear equations. The Computer-Aided Design (CAD) community needs to be ready for this revolutionizing new technology. While research on automatic design methods for quantum computers is currently underway, there is still far too little coordination between the CAD community and the quantum community. Consequently, many CAD approaches proposed in the past have either addressed the wrong problems, or failed to reach the end users. This special session is aiming for addressing these issues by providing talks covering both “sides”: techniques and ideas recently proposed within the CAD domain as well as current solutions and open challenges within the quantum domain.

10A.1 **Computer-Aided Design for Quantum Computation**
Robert Wille - Johannes Kepler Univ. Linz

10A.2 **Classical Programming Challenges on the Road to a Large-Scale Quantum Computer**
Austin Fowler - Google, Inc.

10A.3 **Classical Verification of Quantum Computers**
Yehuda Naveh - IBM Research, Israel

10B - Taming the Wild: Scalable Methods in Verification

**Time:** 3:45 - 5:15pm | **Room:** Monte Carlo

**Moderator:**
Ian Harris - Univ. of California, Irvine

The growing size and complexity of integrated circuits and systems makes scalability of verification solutions an increasingly important problem. This session presents three innovations in this space. The first paper introduces a new theoretical framework for mitigating the verification complexity of large arithmetic circuits. The second paper develops a formal model for the verification of GPU architectures. The third paper presents an emulation platform for mixed-signal systems with high-accuracy and throughput.

10B.1* **PolyCleaner: Clean Your Polynomials Before Backward Rewriting to Verify Million-Gate Multipliers**
Alireza Mahzoon - Universität Bremen
Daniel Große, Rolf Drechsler - Universität Bremen / DFKI

10B.2 **A Formal Instruction-Level GPU Model for Scalable Verification**
Yue Xing, Bo-Yuan Huang, Aarti Gupta, Sharad Malik - Princeton Univ.

10B.3 **Fast FPGA Emulation of Analog Dynamics in Digitally-Driven Systems**
Steven Herbst, Byong Chan Lim, Mark Horowitz - Stanford Univ.

All speakers are denoted in bold | * denotes Best Paper Candidate
10C - Capturing Perturbation for DNN Security

**Time: 3:45 - 5:15pm | Room: Riveria**

**Moderator:**
Wujie Wen - Florida International Univ.

This session showcases advances on DNN security, including watermarking DNNs for IP protection, utilizing sensor pattern noise for detecting adversarial attacks, and a hardware/software co-design framework for enabling online defense against adversarial samples.

**10C.1  SPN Dash – Fast Detection of Adversarial Attacks on Mobile via Sensor Pattern Noise Fingerprinting**
Kent Nixon, Jiachen Mao, Huanrui Yang - Duke Univ.
Juncheng Shen - Zhejiang Univ.
Hai (Helen) Li, Yiran Chen - Duke Univ.

**10C.2  Watermarking Deep Neural Networks for Embedded Systems**
Jia Guo, Miodrag Potkonjak - Univ. of California, Los Angeles

**10C.3  DeepFense: Real-Time Defense against Adversarial Deep Learning**
Bita Darvish Rouhani - Univ. of California, San Diego
Mohammad Samragh Razlighi, Mojan Javaheripi - University of California San Diego
Tara Javidl, Farinaz Koushanfar - Univ. of California, San Diego

All speakers are denoted in bold | * denotes Best Paper Candidate
Special Session 10D - A Hardware Outlook on Machine Learning Applications

*Time: 3:45 - 5:15pm | Room: Capri*

**Moderators:**
- Diana Marculescu - Carnegie Mellon Univ.
- Da-Cheng Juan - Google, Inc.

This session brings together perspectives from industrial and academic viewpoints on the importance of hardware architecture choice on machine learning applications. The first talk addresses the importance of hardware-aware optimized software kernels in achieving energy – and resource – efficient deployment of neural networks (NNs) on IoT edge devices. By augmenting classic NN architecture search techniques with hardware parameters, the second talk addresses the topic of achieving Pareto optimal hardware-aware model configurations for both high-end and mobile platforms. Concluding the session, the third talk discusses hardware-aware power and runtime modeling and optimization techniques that enable NN-hardware platform co-design exploration.

10D.1 **Enabling Deep Learning at the IoT Edge**
Liangzhen Lai, Naveen Suda - Arm, Ltd.

10D.2 **Searching Toward Pareto-Optimal Device-Aware Neural Architectures**
Da-Cheng Juan - Google, Inc.

10D.3 **Hardware-Aware Machine Learning: Modeling and Optimization**

Networking 122 - Networking Reception

*Time: 5:15 - 5:45pm | Room: Frescos Lounge*

Whatever your goal, networking receptions are the perfect venue for you to expand your network and keep you connected! Join us today to catch up with your colleagues and discuss the day's presentations with the conference presenters. All attendees are invited.
THURSDAY SCHEDULE

8:00am - 6:00pm
2nd International Workshop on Quantum Compilation
   Location: Capri

8:00am - 12:00pm
Machine Learning and Systems for Building the Next Generation of EDA Tools
   Location: Monte Carlo

8:15am - 5:00pm
Hardware and Algorithms for Learning On-a-Chip (HALO)
   Location: Marbella/Les Palmas

8:30am - 5:00pm
Top Picks in Hardware Security
   Location: Saint Tropez

8:30am - 4:00pm
International Workshop on Design Automation for Analog and Mixed-Signal Circuit
   Location: Riviera

8:30am - 5:00pm
First Workshop on Open-Source EDA Technology (WOSET)
   Location: Terrazza Ballroom

1:00 - 6:00pm
11th IEEE/ACM Workshop on Variability Modeling and Characterization
   Location: Monte Carlo

Save the Date for ICCAD 2019!
November 4 – 7, 2019
The Westin Westminster
Westminster, CO
2nd International Workshop on Quantum Compilation

**Time:** 8:00am - 6:00pm  |  **Room:** Capri

**Organizers:**
Mathias Soeken - École Polytechnique Fédérale de Lausanne  
Thomas Häner - Eidgenössische Technische Hochschule Zürich

The workshop aims to bring together researchers from quantum computing, electronic design automation, and compiler construction. Open questions that we anticipate this group to tackle include new methods for circuit synthesis and optimization, optimizations and rewriting, techniques for verifying the correctness of quantum programs, and new techniques for compiling efficient circuits and protocols regarding fault-tolerant and architecture constraints.

The scope of the workshop includes, but is not limited to, current hot topics in quantum circuit design such as:

- space-optimizing compilers for reversible circuits
- design-space exploration for automatic code generation from classical HDL specification
- quantum programming languages
- reversible logic synthesis
- technology-aware mapping
- error correction
- optimized libraries (e.g., for arithmetic and Hamiltonian simulation)
- benchmarking of circuits for small and medium scale quantum computers
- quantum and reversible circuit peep-holing and (re)synthesis
- software and tools for all above mentioned topics

**Speakers:**
Alwin Zulehner - Johannes Kepler Univ. Linz  
Gerhard Dueck - Univ. of New Brunswick  
Shin Nishio - Keio Univ.  
Beatrice Nash - Massachusetts Institute of Technology  
Yulu Pan - Keio Univ.  
Giulia Meuli - École Polytechnique Fédérale de Lausanne  
Alan Robertson - The Univ. of Sydney  
Olivia Di Matteo - Univ. of Waterloo  
Eric Peterson - Rigetti Computing  
Mariia Mykhailova - Microsoft Corporation  
Ali Javadi-Abhari - IBM Corp.  
Philipp Niemann - Univ. of Bremen  
Raban Iten - ETH Zurich  
Christophe Chareton - CEA  
Kevin Jin - Sunset High School
Hardware and Algorithms for Learning On-a-Chip (HALO)

**Time:** 8:15am - 5:00pm | **Room:** Marbella/Les Palmas

**Organizers:**
- Jae-sun Seo - Arizona State Univ.
- Yiran Chen - Duke Univ.

In recent years, machine/deep learning algorithms has unprecedentedly improved the accuracies in practical recognition and classification tasks, some even surpassing human-level accuracy. However, to achieve incremental accuracy improvement, state-of-the-art deep neural network (DNN) algorithms tend to present very deep and large models, which poses significant challenges for hardware implementations in terms of computation, memory, and communication. This is especially true for edge devices and portable hardware applications, such as smartphones, machine translation devices, and small wearable devices, where severe constraints exist in performance, power, and area.

There is a timely need to map the latest complex learning algorithms to custom hardware, in order to achieve orders of magnitude improvement in performance, energy efficiency and compactness. Exemplary efforts from industry and academia include many application-specific hardware designs (e.g., Google TPU, FPGA, ASIC, etc.). Recent progress in computational neurosciences and nanoelectronic technology, such as emerging memory devices, will further help shed light on future hardware-software platforms for learning on-a-chip.

The overarching goal of this workshop is to explore the potential of on-chip machine learning, to reveal emerging algorithms and design needs, and to promote novel applications for learning. It aims to establish a forum to discuss the current practices, as well as future research needs in the aforementioned fields.

**Speakers:**
- **Naresh Shanbhag** - Univ. of Illinois at Urbana-Champaign
- **Yangqing Jia** - Facebook
- **Shouyi Yin** - Tsinghua Univ.
- **Lingchuan Meng** - Arm, Ltd.
- **Yanzhi Wang** - Northeastern Univ.
- **Jaeyoun Kim** - Google, Inc.
- **Xiang Chen** - George Mason Univ.
- **Gregory Chen** - Intel Corp.
- **Wei Lu** - Univ. of Michigan
- **Gert Cauwenberghs** - Univ. of California, San Diego
- **Jishen Zhao** - Univ. of California, San Diego

Top Picks in Hardware and Embedded Security

**Time:** 8:30am - 5:00pm | **Room:** Saint Tropez

**Organizers:**
- Ramesh Karri - New York Univ.
- JV Rajendran - Texas A&M Univ.
- Ahmad-Reza Sadeghi - Technische Univ. Darmstadt
- Gang Qu - Univ. of Maryland

Top picks will span a gamut of topics in hardware, micro-architecture, and embedded security. The top picks workshop presentations will be selected from papers that have appeared in leading hardware and embedded security conferences and journals including but not limited to DAC, DATE, ICCAD, HOST, CHES, ETS, VTS, ITC, IEEE S&P, Euro S&P, Usenix Security, ASIA CCS, NDSS, ISCA, MICRO, ASPLOS, HPCA, ACSAC and ACM CCS during the six-year period: 2012 -- 2017. Selected papers from the Top Picks workshop will be invited for submission to an IEEE Transactions on CAD special section on "Top Picks in Hardware and Embedded Security".
First Workshop on Open-Source EDA Technology (WOSET)

**Time:** 8:30am - 5:00pm | **Room:** Terrazza Ballroom

**Organizers:**
Sherief Reda - Brown Univ.
Andrew B. Kahng - Univ. of California, San Diego
Sachin Sapatnekar - Univ. of Minnesota, Twin Cities
Mohamed Shalan - The American Univ. in Cairo

**Background:** The cost and difficulty of IC design in advanced nodes have stifled hardware design innovation and raised unprecedented barriers to bringing new design ideas to the marketplace. Notably, commercial EDA tools have become both expensive and highly complex, as they are aimed at leading-edge, expert users. Unlike the thriving software community, which enjoys a large number of open-source operating systems, compilers, libraries and applications, the hardware community lacks such an ecosystem. While the academic community has produced some high-quality open-source EDA tools in the past (e.g., SPICE and various SAT solvers), the EDA open-source landscape is fragmented and a full open-source EDA flow is lacking. Goal of workshop: This workshop aims to galvanize the open-source EDA movement. The workshop will bring together EDA researchers who are committed to open-source principles to share their experiences and coordinate efforts towards developing a reliable, fully open-source EDA flow. The workshop will feature presentations that overview existing open-source tools, along with a rump session and posters describing future planned EDA tools. The workshop will feature a panel to brainstorm about potential gaps and obstacles to open-source EDA, and how to coordinate efforts and ensure quality and interoperability across open-source tools.

**Submission categories:**
- Overview of an existing open-source EDA tool or planned future tools
- Overview of support infrastructure, such as databases, file formats, and benchmarks.
- Open-source cloud-based tools
- Design-tool interactions
- Position statements (e.g. critical gaps, blockers/obstacles)

**Speakers:**

- Sherief Reda - Brown Univ.
- Andreas Olofsson - Defense Advanced Research Projects Agency
- Andrew B. Kahng - Univ. of California, San Diego
- Sachin Sapatnekar - Univ. of Minnesota, Twin Cities
- Shunning Jiang - Cornell Univ.
- David Fang - Google, Inc.
- Rafael Trapani Possignolo - Univ. of California, Santa Cruz
- Spencer Millican - Auburn Univ.
- Russell Friesenhahn - Univ. of Texas at Austin
- Chun-Xun Lin - Univ. of Illinois at Urbana-Champaign
- Renan Netto - Federal Univ. of Santa Catarina
- Mohamed Shalan - American Univ. of Cairo
- Rainer Doemer - Univ. of California, Irvine
- Bei Yu - Chinese Univ. of Hong Kong
- Gi-Joon Nam - IBM Corp.
- Mathias Soeken - École Polytechnique Fédérale de Lausanne
- Mateus Fogaça - Univ. Federal do Rio Grande do Sul
- Bangqi Xu - Univ. of California, San Diego
- Frank Liu - IBM Corp.
- Jason Verley - Sandia National Laboratories
- Soheil Hashemi - Brown Univ.
- Yi-Shan Lu - Univ. of Texas at Austin
- Jonathan Balkind - Princeton Univ.
- Vaibhav Verma - Univ. of Virginia
- Tsung-Wei Huang - Univ. of Illinois at Urbana-Champaign
- Edward Wang - Univ. of California, Berkeley
- Ross Daly - Stanford Univ.
- Zihao Yuan - Boston Univ.
International Workshop on Design Automation for Analog and Mixed-Signal Circuit

**Time: 8:30am - 4:00pm | Room: Riviera**

**Organizers:**
- Jie Gu - Northwestern Univ.
- Zhuo Feng - Michigan Technological Univ.
- Xin Li - Duke Univ.
- Jaeha Kim - Seoul National Univ.
- Mark Po-Hung Lin - National Chung Cheng Univ.
- Xuan Zeng - Fudan Univ.

A substantial portion of modern integrated circuits are analog and mixed-signal (AMS) circuits that provide critical functionality such as signal conversion. Over the past several decades, aggressive scaling of IC technologies, and the integration of heterogeneous physical domains on a chip, substantially complicates the design of AMS circuits. On the one hand, their modeling and design becomes extremely complex. On the other hand, their interplay with the rest of the system-on-chip challenges design, verification and test. The new technology trends bring enormous challenges and opportunities for AMS design automation. This is reflected by an increase in research activity on AMS CAD worldwide.

Many emerging application brings tremendous new interest in developing analog mixed-signal circuits that accelerate the computing task. Examples include energy efficient neuromorphic computing based analog neurons or memristor devices, time or spiking based circuits for machine learning implementation, resonant based computing or PCM circuits, etc. We will feature this type of new emerging computing methodology in this year’s workshop.

The purpose of this workshop is to bring together academic and industrial researchers from both design and CAD communities to report recent advances and motivate new research topics and directions in this area. Special focuses will be given to the emerging non-traditional analog mixed-signal computing methodology for machine learning, neuromorphic computing.

**Speakers:**
- **Sheriff Sadiqbatcha** - Univ. of California, Riverside
- **David Pan** - Univ. of Texas at Austin
- **Mike Chan** - Univ. of Southern California
- **Peng Li** - Texas A&M Univ.
- **Eric Keiter** - Sandia National Laboratories
- **Zheng Zang** - Univ. of California, Santa Barbara
- **Xiang Chen** - George Mason Univ.
- **Kieth Bowman** - Qualcomm Technologies, Inc.
- **Mingoo Seok** - Columbia Univ.
- **Subhanshu Gupta** - Washington State Univ.
Machine Learning and Systems for Building the Next Generation of EDA Tools

*Time: 8:30am - 12:00pm | Room: Monte Carlo*

**Organizer:**
Claudionor Coelho - Google Inc

This workshop covers the basics of machine learning, systems and infrastructure considerations for performing machine learning at scale, specialized hardware architectures for neural networks, and approaches for using machine learning for building the next generation of EDA tools.

The workshop starts with Naïve Bayes, Support Vector Machines, and Decision Trees, followed by blackbox classifier training with gradient descent. With examples, the workshop illustrates feature selection, model validation and how to avoid overfitting machine learning models. Dimensionality reduction techniques become important for data with high dimensionality for reducing computational and storage requirements. We discuss singular value decomposition (SVD), and principal component analysis (PCA) techniques for dimensionality reduction. Next, the workshop discusses k-means clustering for unsupervised learning, and efficient parallel algorithms for solving this problem for large datasets.

The workshop proceeds on to deep network training and simple convolutional neural networks. It covers common neural net architectures, including ResNet, and Recurrent Neural Networks (RNNs), that are commonly used for many pattern recognition tasks.

We expect participants to build several small EDA based projects using Machine Learning and Deep Learning. Examples of ML/DL small projects that may include, but are not limited to:

1. Data preparation
2. Using regression to perform parameter tuning of EDA heuristics
3. Using k-means clustering to classify heuristics
4. Using convolutional networks to perform feature detection
5. Analyzing traces using recurrent networks or embeddings

Attendees are expected to have basic understanding of Python and Numpy, and have a laptop computer.

**Speakers:**

Claudionor Coelho - Google Inc

Manish Pandey - Synopsys Inc
11th IEEE/ACM Workshop on Variability Modeling and Characterization

**Time: 1:00 - 6:00pm | Room: Monte Carlo**

**Organizers:**
- Rasit Topaloglu - IBM Corp.
- Ibrahim (Abe) M. Elfadel - Masdar Institute of Science and Technology
- Takashi Sato - Kyoto Univ.

This workshop provides a forum to discuss current practices as well as near-future research aimed at addressing the ever-growing problems of variability/reliability and their impact on design performance and cost. The scope of the workshop further covers the detailed technical aspects of variability/reliability characterization, including compact modeling, stochastic simulation, test structure design, statistical CAD, and resilient design. The workshop also provides an opportunity to discuss modeling and characterization needs for emerging device technologies. Compared with other workshops, VMC strives to highlight the existing links among device technology, device physics, device modeling, technology CAD, and related circuit design issues. The topics of the workshop include the following:

- Fundamental device physics and device engineering
- CAD tools: modeling, simulation, and tool integration
- Design interface: design impact and characterisation techniques

In this year’s version of the VMC workshop, the focus will be on three areas that are at the interface between machine learning and variability modeling and characterization.

These areas are:
1. Data Mining for Variability
2. Rare Data and Variability
3. Machine Learning and Variability

Aside from invited presentations on the above three topics, the workshop will also feature poster presentations by the larger community.

**Speakers:**
- **Yiorgos Makris** - Univ. of Texas at Dallas
- **Victor Kravets** - IBM Research
- **Mehdi Tahoori** - Karlsruhe Institute of Technology
- **Youngsoo Shin** - Korea Advanced Institute of Science and Technology
EXECUTIVE COMMITTEE

GENERAL CHAIR
Iris Bahar
School of Engineering
Brown University
182 Hope Street
Providence, RI 02906
401-863-1430 (office)
401-603-6972 (mobile)
iris.bahar@brown.edu

PAST CHAIR
Sri Parameswaran
Univ. of New South Wales
School of Computer Science & Engineering
Sydney, Australia
61296626725
sridevan@cse.unsw.edu.au

PROGRAM CHAIR
David Z. Pan
Dept. of Electrical & Computer Engineering
The Univ. of Texas at Austin
Austin, TX 78712
512-471-1436
dpan@ece.utexas.edu

VICE PROGRAM CHAIR
Yuan Xie
University of California, Santa Barbara
5159 HFH Hall, UCSB
Santa Barbara, CA 93106
805-893-5563
yuanxie@ece.ucsb.edu

TUTORIAL & SPECIAL SESSION CHAIR
Rolf Drechsler
University of Bremen/DFKI
Bibliothekstr. 1, 28359, Bremen, Germany
+49 421 218 63932
drechsle@informatik.uni-bremen.de

WORKSHOP CHAIR
Tulika Mitra
National University of Singapore
School of Computing
13 Computing Drive
Singapore 117417
tulika@comp.nus.edu.sg

EUROPEAN REPRESENTATIVE
Ulf Schlichtmann
Technical University of Munich
Institute for EDA
Arcisstr. 21, Muenchen, Germany
80333 +49 89 289 23665
ulf.schlichtmann@tum.de

ASIAN REPRESENTATIVE
Shih-Chieh Chang
National Tsing Hua University
Dept. of Computer Science
Hsin-Chu, Taiwan, R.O.C.
scchang@cs.nthu.edu.tw

ACM/SIGDA REPRESENTATIVE
Yiran Chen
Dept. of Electrical and Computer Engineering, Duke University
Box 90291
Durham, NC 27708
919-660-5252
yiran.chen@duke.edu

INDUSTRY LIAISON
Patrick Groeneveld
Cadence Design Systems, Inc.
2655 Seely Ave.
San Jose, CA 95134
patrickgroeneveld1@gmail.com

CONFERENCE PLANNER & REGISTRATION MANAGER
Nannette Jordan
MP Associates, Inc.
1721 Boxelder St., Ste. 107
Louisville, CO 80027
303-530-4562
Nannette@mpassociates.com

CEDA REPRESENTATIVE
Gi-Joon Nam
IBM T.J. Watson Research Center
1101 Kitchawan Rd
Yorktown Heights, NY 10598
512-286-7713
gnam@us.ibm.com

ACM/SIGDA REPRESENTATIVE
Yiran Chen
Dept. of Electrical and Computer Engineering, Duke University
Box 90291
Durham, NC 27708
919-660-5252
yiran.chen@duke.edu

EUROPEAN REPRESENTATIVE
Ulf Schlichtmann
Technical University of Munich
Institute for EDA
Arcisstr. 21, Muenchen, Germany
80333 +49 89 289 23665
ulf.schlichtmann@tum.de

ASIAN REPRESENTATIVE
Shih-Chieh Chang
National Tsing Hua University
Dept. of Computer Science
Hsin-Chu, Taiwan, R.O.C.
scchang@cs.nthu.edu.tw

INDUSTRY LIAISON
Patrick Groeneveld
Cadence Design Systems, Inc.
2655 Seely Ave.
San Jose, CA 95134
patrickgroeneveld1@gmail.com

CONFERENCE PLANNER & REGISTRATION MANAGER
Nannette Jordan
MP Associates, Inc.
1721 Boxelder St., Ste. 107
Louisville, CO 80027
303-530-4562
Nannette@mpassociates.com

CEDA REPRESENTATIVE
Gi-Joon Nam
IBM T.J. Watson Research Center
1101 Kitchawan Rd
Yorktown Heights, NY 10598
512-286-7713
gnam@us.ibm.com
Hussam Amrouch
Karlsruhe Institute of Technology

Aydın Aysu
North Carolina State University

Yongchan Ban
Synopsys

Lars Bauer
Karlsruhe Institute of Technology

Kia Bazargan
University of Minnesota

Laleh Behjat
University of Calgary

Davide Bertozzi
University of Ferrara

Philip Brisk
University of California, Riverside

Ro Cammarota
Qualcomm Technologies Inc.

Arquimedes Canedo
Siemens Corporation

Aiqun Cao
Synopsys

Luca Carloni
Columbia University

Mario R. Casu
Politecnico di Torino

Koushik Chakraborty
Utah State University

Deming Chen
UIUC

Yiran Chen
Duke University

Chung-Kuan Cheng
UCSD

Jayita Das
Intel Corp.

Sabya Das
Synopsys Inc.

Marco Donato

Harvard University

Jennifer Dworak
Southern Methodist University

Deliang Fan
University of Central Florida

Yunsi Fei
Northeastern University

Farshad Firouzi
imec/KU Leuven

Tony Givargis
University of California, Irvine

Joel Grodstein
Tufts University

Jie Gu
Northwestern University

Jie Han
University of Alberta

Yuko Hara-Azumi
Tokyo Institute of Technology

Ian Harris
University of California Irvine

Christopher Harris
Auburn University

Tsung-Yi Ho
National Tsing Hua University

Christian Hochberger
TU Darmstadt

William Hung
Synopsys

Wooyoung Jang
Dankook University

Dan Jiao
Purdue University

Yier Jin
University of Florida

Kerim Kalafala
IBM

Timothy Kam
Intel

Nagaraj Kelageri
Qualcomm

Michel Kinsky
Boston University

Christoph M. Kirsch
University of Salzburg

Yukihide Kohira
The University of Aizu

Farinaz Koushanfar
University of California San Diego

Jaydeep Kulkarni
University of Texas at Austin

Liangzhen Lai
Arm Inc.

Hsien-Hsin Lee
TSMC

Wenchao Li
Boston University

Jin-Fu Li
National Central University

Huawei Li
Chinese Academy of Sciences

Yun (Eric) Liang
Peking University

Yibo Lin
University of Texas at Austin

Jai-Ming Lin
National Cheng Kung University

Mark Po-Hung Lin
National Chung Cheng University

Wen-Hao Liu
Cadence Design Systems

Ken Mai
CMU

Igor L. Markov
University of Michigan

Dmitri Maslov
National Science Foundation

Brett Meyer
McGill University
TECHNICAL PROGRAM COMMITTEE

Prabhat Mishra  
University of Florida

Tulika Mitra  
National University of Singapore

Kartik Mohanram  
University of Pittsburgh

Alessandra Nardi  
Cadence Design Systems

Nicola Nicolici  
McMaster University

Umit Ogras  
Arizona State University

Hamed Okhravi  
MIT Lincoln Laboratory

Mustafa Ozdal  
Bilkent University

Sule Ozev  
ASU

David Z. Pan  
University of Texas at Austin

Harindranath Parameswaran  
Cadence Design Systems

Jongsun Park  
Korea University

Sudeep Pasricha  
Colorado State University

Weikang Qian  
Shanghai Jiao Tong University

Jeyavijayan Rajendran  
Texas A&M University

Sandip Ray  
Univ. of Florida

Arijit Raychowdhury  
University of California at Berkeley

Sherief Reda  
Brown University

Francesco Regazzoni  
ALoRI

Haoxing Ren  
NVIDIA Corporation

Gabriel Rutsch  
Infineon Technologies AG

Ahmad-Reza Sadeghi  
Technische Universitaet Darmstadt

Fareena Saqib  
fsaqib@uncc.edu

John Sartori  
University of Minnesota

Takashi Sato  
Kyoto University

Ioannis Savidis  
Drexel University

Shreyas Sen  
Purdue University

Jae-sun Seo  
Arizona State University

Zili Shao  
Hong Kong Polytechnic University

Yiyu Shi  
University of Notre Dame

Mathias Soeken  
EPFL

Mircea Stan  
University of Virginia

Phillip Stanley-Marbell  
MIT

Valery Sukharev  
Mentor Graphics Corporation

Susmita SurKolay  
INDIAN STATISTICAL INSTITUTE

Sheldon Tan  
University of California at Riverside

Shobha Vasudevan  
UIUC

Miroslav N. Velev  
Aries Design Automation

Ingrid Verbaaewhede  
KU Leuven - COSIC

Ting-Chi Wang  
National Tsing Hua University

Yanzhi Wang  
University of Southern California

Sheng Wei  
University of Nebraska

Wujie Wen  
Florida International University

Yuan Xie  
University of California, Santa Barbara

JinJun Xiong  
IBM T.J. Watson Research

Xiaqing Xu  
Arm Inc.

Chia-Lin Yang  
National Taiwan University

Chengmo Yang  
University of Delaware

Yang (Cindy) Yi  
Virginia Tech

Shouyi YIN  
Tsinghua University

Bei Yu  
Chinese University of Hong Kong

Hao Yu  
Nanyang Technological University

Shimeng Yu  
Arizona State University

Bo Yuan  
City University of New York

Xuan Zeng  
Fudan University

Zhiyu Zeng  
Cadence Design Systems

Wei Zhang  
Hong Kong University of Science and Technology

Zheng Zhang  
University of California, Santa Barbara

Jishen Zhao  
UC San Diego

Pingqiang Zhou  
ShanghaiTech University

Cheng Zhuo  
Zhejiang University
About ACM

ACM, the Association for Computing Machinery, acm.org, is the world’s largest educational and scientific computing society, uniting computing educators, researchers and professionals to inspire dialogue, share resources and address the field’s challenges. ACM strengthens the computing profession’s collective voice through strong leadership, promotion of the highest standards, and recognition of technical excellence.

ACM supports the professional growth of its members by providing opportunities for life-long learning, career development, and professional networking. ACM provides the computing field’s premier Digital Library (DL), an invaluable online resource of over two million fully searchable pages of text, including a 50+ year archive, from ACM’s high quality journals and proceedings. The DL also reaches the entire world of computing through the fully integrated Guide to Computing Literature. ACM’s 37 Special Interest Groups (SIGs) focus on different computing disciplines. More than half of all ACM members join one or more of these Special Interest Groups. The SIGs publish newsletters and sponsor important conferences such as SIGGRAPH, SPLASH including OOPSLA, DAC, ICCAD and CHI, giving members opportunities to meet experts in their fields of interest and network with other knowledgeable members.

Become an ACM member today and join thousands of other leading professionals, researchers and academics who benefit from all ACM has to offer. Join ACM online at acm.org, or contact ACM directly by phone: 800-342-6626 (US and Canada) or 212-626-0500 (Global), by fax: 212-944-1318, or by e-mail: acmhelp@acm.org.

Join ACM/SIGDA: The Resource For EDA Professionals

ACM/SIGDA, (Special Interest Group on Design Automation) provides a broad array of resources to our members, to students, professors, industry professionals and, to the EDA field in general. SIGDA sponsors various events to promote interaction among the community to share the latest technical and professional advances. It also serves as a forum to support events that nurture new ideas and infuse vitality into new emerging trends in the field.

SIGDA has a long history of supporting conferences and the EDA profession including ICCAD, DAC, DATE, and ASP-DAC, plus around 15 focused symposia and workshops. SIGDA supports various events such as - the University Research Demonstration that helps to foster interactions between students and industry; Design Automation Summer School that exposes students to trending topics; Young Faculty Workshops; Ph.D. Forums in conjunction with major conferences, design contests such as CAD Athlon. SIGDA funds various scholarships and recognizes outstanding research publications. Awards recognize significant contributions at all stages of the professional career from student awards to the Pioneer Award for Lifetime achievement. SIGDA has launched new programs such as SIGDA Live, a series of monthly webinars on topics of general interest to the SIGDA community and a more global E-Newsletter with a newly formed editorial board. SIGDA also supports local chapters that help with professional networking. SIGDA also administers Student Research Competition on behalf of ACM.

SIGDA pioneered electronic publishing of EDA literature, beginning with the DA Library in 1989. SIGDA also provides strong support for the ACM journal TODAES (Transactions on Design Automation of Electronic Systems). Major benefits provided to SIGDA members include free access to all SIGDA sponsored publications in the ACM Digital Library, and reduced registration rates for SIGDA sponsored events.

For further information on SIGDA’s programs and resources, see sigda.org.

Please join us in building a more vibrant community and volunteer for SIGDA.
IEEE is the world’s largest professional association dedicated to advancing technological innovation and excellence for the benefit of humanity. IEEE and its members inspire a global community through IEEE’s highly cited publications, conferences, technology standards, and professional and educational activities.

IEEE Council on Electronic Design Automation (CEDA)


For more information on CEDA, visit: ieee-ceda.org.

CAS

The IEEE Circuits and Systems Society’s field of interest spans the theory, analysis, design (computer aided design), and practical implementation of circuits, and the application of circuit theoretic techniques to systems and to signal processing. The coverage of this field includes the spectrum of activities from, and including, basic scientific theory to industrial applications.

The IEEE Circuits and Systems Society (CASS) believes that the Grand Engineering Challenges of the 21st century can only be addressed in an inter-disciplinary and cross-disciplinary manner. The Society’s unique and profound expertise in Circuits, Systems, Signals, Modeling, Analysis, and Design can have a decisive impact on important issues such as Sustainable Energy, Bio-Health, Green Information Technology, Nano-Technology, and Scalable Information Technology Systems.

Our mission is to foster CASS members across disciplines to address humanity’s grand challenges by conceiving and pioneering solutions to fundamental and applied problems in circuits and systems.
The IEEE Electron Devices Society (EDS) is involved in the advancement of electronics and electrical engineering through research, development, design, manufacture, materials, and applications of electron devices. EDS is concerned with technical, educational, scientific publication and meeting activities which provide benefits to members while contributing towards the progress of this field. eds.ieee.org.

Thank You to our Technical Program Dinner Corporate Sponsor • • •

cadence®
ACADEMIC NETWORK

Conference Sponsor Recognition

TPC Dinner and Monday Evening Reception, November 5
cadence®
ACADEMIC NETWORK

Coffee Breaks on Tuesday, November 6

Tuesday Evening Reception, November 6

huawei

synopsys®
Silicon to Software®
Hilton San Diego Resort & Spa

Hotel Layout