<table>
<thead>
<tr>
<th>TIME</th>
<th>ALMADEN BALLROOM</th>
<th>ALMADEN 1</th>
<th>ALMADEN 2</th>
<th>WINCHESTER</th>
<th>MARKET 1 &amp; 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>8:30 - 9:30am</td>
<td>Keynote Address: What Role Can Hardware Design Play in Cybersecurity? Srinivas Devadas, Massachusetts Institute of Technology</td>
<td>Fast Track: Wednesday Regular Paper Presentations</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9:30 - 10:00am</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10:30am - 12:00pm</td>
<td>Session 7A: Approximate and Stochastic Circuits</td>
<td>Session 7B: Cool Technologies for Cool Chips</td>
<td>Session 7C: Design and CAD to Enable 3D Integration</td>
<td>Designer Track 7D: DFM for Extreme Technology Nodes</td>
<td></td>
</tr>
<tr>
<td>12:00 - 1:00pm</td>
<td>Lunch: Hyatt Hotel - Grand Hall</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1:30 - 3:30pm</td>
<td>Embedded Tutorial 8A: Automated and Quality-Driven Requirement Engineering</td>
<td>Special Session 8B: Pessimism Removal During Timing Analysis</td>
<td>Session 8C: Emulation, Modeling and Simulation of Analog Systems</td>
<td>Session 8D: Advanced Placement</td>
<td></td>
</tr>
<tr>
<td>4:00 - 5:30pm</td>
<td>Special Session 9A: Advances in Debug and Formal Verification</td>
<td>Session 9B Mathematical Methods for Interconnect Modeling and Low Power Design</td>
<td>Session 9C: Software for Management of Parallelism and Data Integrity in Embedded Systems</td>
<td>Session 9D: Clock Network Design and Timing</td>
<td></td>
</tr>
<tr>
<td>5:30 - 6:00pm</td>
<td>Networking Reception: Almaden Foyer</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Nary a day goes by without hearing about break-ins into software systems, with personal or confidential data being compromised. Yet, as time goes on, we are trusting the cloud more and more to perform sensitive operations for us. "Emanding" more trust in software systems appears to be a recipe for disaster.

Can hardware rescue us? Suppose we only trust hardware manufacturers and cryptographers, and not system software developers, application programmers, or other software vendors. It will be the hardware manufacturer’s job to produce a piece of hardware that provides some security properties. The additional physical security that comes with hardware is a bonus; however, there is still a leap of faith! We must trust that the hardware’s security guarantees really do take software out of the loop.

This poses a challenging problem. Software that operates on our data is assumed to be curious or malicious. To make matters worse, the cloud service provider can also be malicious and can run whatever program it wants on our data. How can we ensure privacy of data despite the practically infinite number of malicious programs out there? In this talk, processor architectures being developed in academia and industry will be described that are attempting to address cybersecurity and privacy challenges through innovative hardware design.

**Biography:** Srinivas Devadas is the Webster Professor of Electrical Engineering and Computer Science at the Massachusetts Institute of Technology (MIT). He received his MS and PhD from the Univ. of California, Berkeley in 1986 and 1988, respectively. He joined MIT in 1988 and served as Associate Head of the Department of Electrical Engineering and Computer Science, with responsibility for Computer Science, from 2005 to 2011. Devadas’s research interests span Computer-Aided Design (CAD), computer security and computer architecture. In CAD, his work on logic synthesis and power estimation resulted in several best paper awards at the Design Automation Conference and in IEEE Transactions. Devadas was elected a Fellow of the IEEE in 1999 for contributions to design automation. He received the IEEE Computer Society Technical Achievement Award in 2014 for inventing Physical Unclonable Functions and single-chip secure processor architectures. Devadas’s work on hardware information flow tracking published in the 2004 ASPLOS received the ASPLOS Most Influential Paper Award in 2014.
This session presents innovations in approximate and stochastic circuits. Approximate circuits allow precision to be trade-off for improvements in area, delay and power. Stochastic circuits use random bitstreams to encode values -- the value encoded is the probability any given bit of the stream is 1. The first paper describes multi-level logic synthesis techniques for approximate circuits that handle user-provided constraints on error magnitudes and frequency. The second paper describes models for the error characteristics of approximate adders and presents a new approximate adder design. The last paper offers an approach to reduce the silicon area required to generate multiple stochastic bitstreams having different probabilities.

**7A.1 Multi-Level Approximate Logic Synthesis Under General Error Constraints**
Jin Miao, Andreas Gerstlauer, Michael Orshansky - Univ. of Texas at Austin

**7A.2 On Error Modeling and Analysis of Approximate Adders**
Li Li - Synopsys, Inc., Inc.
Hai Zhou - Northwestern Univ.

**7A.3 Generating Multiple Correlated Probabilities for MUX-Based Stochastic Computing Architecture**
Yili Ding, Yi Wu, Weikang Qian - Shanghai Jiao Tong Univ.
This session focuses on the design and CAD skills for emerging vertical structures. The first paper discusses a layout CAD flow for vertical channel devices. The second paper talks how to efficiently integrate photonic ring resonators in the vertical structure and alleviate the thermal issue. The third paper expands the discussion to full chip power delivery network in 3D ICs.

**7C.1 Efficient Layout Generation and Evaluation of Vertical Channel Devices**
Wei-Che Wang, Puneet Gupta - Univ. of California, Los Angeles

**7C.2 Thermal-Aware Synthesis of Integrated Photonic Ring Resonators**
Christopher Condrat - Calypto Design Systems, Inc.
Priyank Kalla, Steve Blair - Univ. of Utah

**7C.3 Full Chip Impact Study of Power Delivery Network Designs in Monolithic 3D ICs**
Sandeep Kumar Samal - Georgia Institute of Technology
Kambiz Samadi, Pratyush Kamal, Yang Du - Qualcomm Technologies, Inc.
Sung Kyu Lim - Georgia Institute of Technology

As the technology approaches 10nm process nodes and beyond, complex Design-for-Manufacturability techniques and processes have to be adopted to ensure the correctness and yield of the semiconductor product. In this designer track session, three industrial presenters will describe the challenges and solutions from different perspectives.

**7D.1 Evolving Physical Design Paradigms in the Transition from 20/14 to 10nm Process Technology Nodes**
Luigi Capodieci - GLOBALFOUNDRIES

**7D.2 Design and Manufacturing Process Co-optimization in Nano-Technology**
Meng-Kai Hsu, Nitesh Katta, Tzu-Hen Lin, Yen-Hung Lin, King Ho Tam, Chung-Hsing Wang - Taiwan Semiconductor Manufacturing Co., Ltd.

**7D.3 Design and Technology Co-Optimization Near Single-Digit Nodes**
Lars Liebmann, Rasit Topaloglu - IBM Corp.
The design flow for complex safety critical systems starts way before the implementation phase. A considerate amount of time is spent on extracting and organizing requirements from several documents that are provided by the stakeholders and customers. This process is called requirement engineering and usually carried out manually thus far. Some software tools, in particular IBM Rational DOORS1, are available that mainly focus on providing methods to organize requirements and link them to artifacts of the design flow. Besides extracting and organizing requirements, designers also link them to model elements, code blocks, and verification plans such they can be traced during the implementation phase. In this tutorial, we present (automatic) methods which ease this flow, i.e. (i) analysis schemes checking whether requirements are indeed formulated according to proper guidelines, (ii) automatic approaches for the extraction of requirements from customer specifications, and (iii) verification methods that check the extracted requirements for consistency. Natural language processing tools and formal methods are used for this purpose.

8A.1 Automated and Quality-Driven Requirement Engineering
Rolf Drechsler, Mathias Soeken, Robert Wille - Univ. of Bremen

8B Special Session: Pessimism Removal During Timing Analysis
Room: Almaden 2
Moderator: Jin Hu - IBM Corp.

Static timing analysis is a key component of any integrated circuit (IC) chip design closure flow, and is employed (i) to obtain bounds on the fastest (early) and slowest (late) signal transition times for various timing tests and paths and (ii) drive various physical synthesis and physical design optimizations. Growing chip design sizes and complexities (e.g., increased number of clock domains, increased significance of crosstalk coupling, voltage islands), as well as more complex and accurate timing models (e.g., current source models) lead to longer timing analysis run-times, thereby hindering designer productivity.

Trade-offs are naturally performed on timing model complexity to achieve practical turnaround-times for chip static timing analysis. To margin against the ignored (or traded-off or uncertain) modeling limitations that are not explicitly and accurately modeled in the native timing models, early and late signal propagation delays (for both gates and wires) are made further pessimistic by the addition of extra guard bands. While these forced early-late splits provide the desired safety margins, applying the splits for the full path of some timing test introduces excessive and undesired pessimism if the data path shares an overlap with the clock path. Common path pessimism removal (CPPR) attempts to remove this pessimism by tracing these potentially problematic paths and discarding some of the early-late difference along the common sub-path. This session will showcase the techniques and methods used by the top-performing contestants of the TAU 2014 Timing Contest to perform CPPR.

8B.1 TAU 2014 Contest on Removing Common Path Pessimism during Timing Analysis

8B.2 Common Path Pessimism Removal: An Industry Perspective
Vibhor Garg - Cadence Design Systems, Inc.

8B.3 Fast Path-Based Timing Analysis for CPPR
Tsung-Wei Huang, Pei-Ci Wu, Martin D.F. Wong - Univ. of Illinois at Urbana-Champaign

8B.4 iTimerC: Common Path Pessimism Removal Using Effective Reduction Methods
Yu-Ming Yang, Yu-Wei Chang, Iris Hui-Ru Jiang - National Chiao Tung Univ.

8B.5 TKtimer: Fast & Accurate Clock Network Pessimism Removal
Christos Kalonakis, Charalampos Antoniadis, Panagiotis Giannakou, Dimos Diooudis - Univ. of Thessaly, George Pinitas - Delft Univ. of Technology, George Stamoulis - Univ. of Thessaly


**8C**

**Emulation, Modeling and Simulation of Analog Systems**

**Room: Winchester**

**Moderators:**
- Ting Mei - Sandia National Labs
- Jaijeet Roychowdhury - Univ. of California, Berkeley

The first two papers present formulations for analysing the steady-state and transient behavior of oscillatory systems. The third paper describes a technique for embedding high-frequency nonidealities in a standard BSIM model using measurement data. The final paper describes a technique for mapping behavioral models of AMS systems onto FPGAs for fast emulation.

**8C.1 A Novel Linear Algebra Method for the Determination of Periodic Steady States of Nonlinear Oscillators**

Haotian Liu, Kim Batselier, Ngai Wong - Univ. of Hong Kong

**8C.2 A Unifying and Robust Method for Efficient Envelope-Following Simulation of PWM/PFM DC-DC Converters**

Ya Wang, Peng Li, Suming Lai - Texas A&M Univ.

**8C.3 Large-Signal MOSFET Modeling Using Frequency-Domain Nonlinear System Identification**

Moning Zhang, Yang Tang, Zuochang Ye - Tsinghua Univ.

**8C.4 Pragma-Based Floating-to-Fixed Point Conversion for the Emulation of Analog Behavioral Models**


---

**8D**

**Advanced Placement**

**Room: Market 1 & 2**

**Moderators:**
- Ismail Bustany - Mentor Graphics Corporation
- Martin D.F. Wong - Univ. of Illinois at Urbana-Champaign

In this session, we have four interesting papers on circuit placement. The first one gives a Lagrangian Relaxation method to solve the asynchronous circuit placement problem. The second one is on large scale FPGA packing and placement. The third paper is placement for regularity. The last one is power clamp placement for ESD protection.

**8D.1 Asynchronous Circuit Placement by Lagrangian Relaxation**

Gang Wu, Tao Lin - Iowa State Univ.
Hsin-Ho Huang - Univ. of Southern California
Chris Chu - Iowa State Univ.
Peter Beerel - Univ. of Southern California

**8D.2 Efficient and Effective Packing and Analytical Placement for Large-Scale Heterogeneous FPGAs**

Yu-Chen Chen - National Taiwan Univ.
Sheng-Yen Chen - National Chiao Tung Univ.
Yao-Wen Chang - National Taiwan Univ.

**8D.3 A Hierarchical Approach for Generating Regular Floorplans**

Javier De San Pedro, Jordi Cortadella, Antoni Roca - Univ. Politècnica de Catalunya

**8D.4 Planning and Placing Power Clamps for Effective CDM Protection**

Hsin-Chun Lin - National Chiao Tung Univ. and Global Unichip Corp.
Shih-Ying Liu, Hung-Ming Chen - National Chiao Tung Univ.
9A | Special Session: Advances in Debug and Formal Verification
---
**Moderator:**
Yirng-An Chen - Marvell Semiconductor, Inc.

**Organizer:**
Miroslav Velev - Aries Design Automation, LLC

The four papers in the session present recent advances in debug and formal verification. The first paper, entitled “On Application of Data Mining Methods in Functional Debug,” investigates the use of data mining in functional debug of microprocessors. The second paper, entitled “Improving the Efficiency of Automated Debugging of Pipelined Microprocessors by Symmetry Breaking in Modular Schemes for Boolean Encoding of Cardinality,” presents a method for symmetry breaking when encoding cardinality constraints in debug of pipelined microprocessors that are formally verified by Correspondence Checking and exploiting the property of Positive Equality. The third paper, entitled “Multiple Clock Domain Synchronization in a QBF-based Verification Environment,” introduces a novel framework for verifying designs with multiple clocks using Quantified Boolean satisfiability (QBF). The fourth paper, entitled “Probabilistic Model Checking for Comparative Analysis of Automated Air Traffic Control System Configurations,” explores techniques for probabilistic model checking of the Automated Airspace Concept (AAC) system.

9A.1 | On Application of Data Mining in Functional Debug
---
Kuo-Kai Hsieh, Wen Chen, Li-C. Wang - Univ. of California, Santa Barbara
Jayanta Bhadra - Freescale Semiconductor, Inc.

9A.2 | Improving the Efficiency of Automated Debugging of Pipelined Microprocessors by Symmetry Breaking in Modular Schemes for Boolean Encoding of Cardinality
---
Miroslav Velev, Ping Gao - Aries Design Automation, LLC

9A.3 | Multiple Clock Domain Synchronization in a QBF-Based Verification Environment
---
Djordje Maksimovic, Bao Le, Andreas Veneris - Univ. of Toronto

9A.4 | Probabilistic Model Checking for Comparative Analysis of Automated Air Traffic Control System
---
Yang Zhao - Microsoft Corp.
Kristin Yvonne Rozier - NASA

9B | Mathematical Methods for Interconnect Modeling and Low Power Design
---
**Room:** Almaden 2

**Moderators:**
Wenjian Yu - Tsinghua Univ.
Eli Chiprout - Intel Corp.

This session contains papers addressing mathematical methods in the areas of interconnect modeling and low power design. The first paper develops a nonlinear zonotoped macromodel for verifying high-speed I/O links under variations, able to generate worst-case eye diagram parameters with small error and much faster than Monte Carlo. The second paper addresses accurate parasitic extraction for high-density cylindrical ITVs by efficient techniques based on the floating random walk method, consuming much less memory than Monte Carlo methods. The third paper presents a self-learning methodology leading to optimal configurations for channel-adaptive process-resilient low-power MIMO front-ends.

9B.1 | A Zonotoped Macromodeling for Reachability Verification of Eye-Diagram in High-Speed I/O Links with Jitter
---
Sai Manoj PD, Hao Yu - Nanyang Technological Univ.
Chenji Gu, Cheng Zhuo - Intel Corp.

9B.2 | Random Walk Based Capacitance Extraction for 3D ICs with Cylindrical Inter-Tier-Vias
---
Wenjian Yu, Chao Zhang, Qing Wang - Tsinghua Univ.
Yiyu Shi - Missouri Univ. of Science and Technology

---
Debashis Banerjee, Barry Muldrey - Georgia Institute of Technology
Shreyas Sen - Intel Corp.
Xian Wang, Abhijit Chatterjee - Georgia Institute of Technology
Software for Management of Parallelism and Data Integrity in Embedded Systems
Room: Winchester

**Moderator:**
Jose Ayala - Complutense Univ. of Madrid

This session tackles the problem of managing the parallel execution and the data integrity issues in embedded systems by means of novel software techniques. The first paper proposes a context-switch-enabled pipelining approach for the synthesis of data-parallel kernels. It formulates a scheduling problem for minimizing the context-switching cost of the multithreaded pipeline with an exact formulation and an efficient heuristic to solve the optimization problem. The second paper extends previously proposed analytical modeling techniques in the field of floating-point to fixed-point conversion to a larger class of programs. This approach extracts a compact, graph-based representation of the program. Finally, it is presented a warranty-aware page management design to mitigate the operation overhead required for managing the endurance issue in PCM-based embedded systems.

**9C.1 Multithreaded Pipeline Synthesis for Data-Parallel Kernels**
Mingxing Tan - Cornell Univ.
Bin Liu - Micron Technology, Inc.
Steve Dai, Zhiru Zhang - Cornell Univ.

**9C.2 Toward Scalable Source Level Accuracy Analysis for Floating-Point to Fixed-Point Conversion**
Gaël Deest - Univ. of Rennes 1
Tomofumi Yuki - INRIA
Olivier Sentieys - INRIA, Univ. of Rennes 1
Steven Derrien - Univ. of Rennes 1

**9C.3 Warranty-Aware Page Management for PCM-Based Embedded Systems**
Sheng-Wei Cheng - National Taiwan Univ.
Yu-Fen Chang - National Tsing Hua Univ.
Yuan-Hao Chang - Academia Sinica
Hsin-Wen Wei - Tamkang Univ.
Wei-Kuan Shih - National Tsing Hua Univ.

Clock Network Design and Timing
Room: Market 1 & 2

**Moderators:**
Rajendra Panda - Oracle Corp.
Tao Huang - Synopsys, Inc., Inc.

Improving the accuracy of Static Timing Analysis (STA) through EDA advancements in Common Path Pessimism Removal (CPPR), and improving the generation and distribution of clocks through resonant clocking, are presented in this session. Two types of resonant clocking, rotary and coupled LC, are featured in the first two papers. An EDA solution to integrating CPPR into the STA flow for improved accuracy is presented in the third paper.

**9D.1 Frequency-Centric Resonant Rotary Clock Distribution Network Design**
Ying Teng, Baris Taskin - Drexel Univ.

**9D.2 Opportunistic Through-Silicon-Via Inductor Utilization in Resonant Clock: Concept and Algorithms**
Umamaheswara Rao Tida - Missouri Univ. of Science and Technology
Varun Mittapalli - Missouri Univ. of Science and Technology
Cheng Zhuo - Intel Corp.
Yiyu Shi - Missouri Univ. of Science and Technology

**9D.3 UI-Timer: An Ultra-Fast Clock Network Pessimism Removal Algorithm**
Tsung-Wei Huang, Pei-Ci Wu, Martin D.F. Wong - Univ. of Illinois at Urbana-Champaign