Welcome to the 34th edition of the IEEE/ACM International Conference on Computer-Aided Design! ICCAD is the premier forum to explore emerging technology challenges, present cutting-edge R&D solutions, record theoretical and empirical advances, and identify future roadmaps for design automation. Continuing a long tradition, ICCAD continues to be the home for the ACM/SIGDA CADathlon and Student Research Competition, several CAD contests, including the IEEE CEDA CAD Contest, and a remarkable set of workshops on design automation for analog and mixed-signal circuits, EDA research on learning on a chip, design for dark silicon era, variability modeling and characterization, and formal verification.

The technical program of the conference is the result of a competitive selection process. The program committee received 382 worldwide submissions for review by 118 outstanding TPC members organized into 18 subcommittees. Our rigorous double-blind review process culminated with an all-day in-person meeting for the entire TPC in San Francisco where only 94 regular papers were selected for inclusion. This marks a record number of submissions and competitive selection process of only a 24.6% acceptance rate.

In addition to the 26 regular paper sessions, the program features four keynote talks, one Designer Track session, one Embedded Tutorial, eleven special sessions, and one collocated Wednesday evening panel hosted by Synopsys. The scope of presentations included in the program spans all aspects of modern problems in design automation, with a forward-looking coverage of hardware security, smart buildings, statistical learning on silicon, and smart hardware acceleration. Continuing last year’s tradition, we hope you will join us every morning for the fast track session charting the day with a mini preview of the presentations to come.

This year marks the fourteenth edition of the SIGDA CADathlon competition which, every Sunday at ICCAD, gathers the brightest minds in design automation for a one-day of full speed coding for EDA. Join us on Monday morning to find out who the winners are! For several years, ICCAD has been the venue for hosting the IEEE CEDA/Taiwan Ministry of Education CAD Contest. This year the contest problems on 3D IC design and optimization, equivalence checking, and timing-driven placement attracted 112 participating teams worldwide, the largest on record. The contest results are announced during the Monday evening contest session, along with the release of contest benchmarks. Joining this tradition, the TAU contest on incremental timing analysis and the IEEE Rebooting Computing Challenge for Low Power Image Recognition will also present the problems and best results in their categories. Please join the contestants and problem proposers on Monday evening for presentations and networking with your peers.

We are fortunate to host several distinguished keynote speakers this year: the Monday morning keynote is by Lydia Kavraki, Harding Professor of Computer Science at Rice University, on the connections between robotics, bioinformatics, and design automation. An additional Monday luncheon keynote is presented by Chuck Alpert, Senior Architect at Cadence Design Systems on unexpected applications of logic synthesis to NCAA gaming. On Tuesday, the IEEE CEDA Luncheon Distinguished Lecture is presented by Steve Keckler, Senior Director of Architecture Research at NVIDIA. Renu Mehra, R&D Director at Synopsys, will give the final keynote of the conference on Wednesday morning on the importance of energy efficient computing in the presence of emerging applications and technologies. We hope that these keynotes, together with the rest of the conference, will make ICCAD the ultimate destination for all design automation practitioners and researchers.

We are grateful to our ICCAD 2015 sponsors and supporters for making this conference another successful event. Enjoy ICCAD in Austin!

Diana Marculescu, ICCAD 2015 General Chair
Carnegie Mellon University, Dept. of Electrical and Computer Engineering
- FOR SPEAKERS & PRESENTERS -

SPEAKERS’ BREAKFAST
Please attend the day of your presentation!

Room: Phoenix North
Monday, November 2 7:00am - 8:00am
Tuesday, November 3 8:00am - 9:00am
Wednesday, November 4 7:00am - 8:00am

NEED PRACTICE?
The DeWitt and Robertson rooms are available and are set up with a computer, LCD projector and screen to view your slides before your session.

Room: DeWitt and Robertson
Monday, November 2 7:00am - 6:00pm
Tuesday, November 3 7:00am - 6:00pm
Wednesday, November 4 7:00am - 4:00pm

- ICCAD SOCIAL MEDIA -
Connect with ICCAD through Twitter @ICCAD. ICCAD will be tweeting hourly updates and conference highlights!

Find ICCAD on LinkedIn and keep up to date with the latest news and insights.

- REGISTRATION HOURS & LOCATION -

Room: Prefunction Central
Monday, November 2 7:00am – 6:00pm
Tuesday, November 3 7:00am – 6:00pm
Wednesday, November 4 7:00am – 6:00pm
Thursday, November 5 7:00am – 6:00pm
Friday, November 6 7:00am – 10:00am

- PARKING INFORMATION -
Attendees receive complimentary day use self-parking and $5.00/day overnight self-parking at the DoubleTree by Hilton Austin.

- CONFERENCE MANAGEMENT -
Our mission is to facilitate networking, education and marketing with efficiency and precision in order to maximize customer experiences, and client profitability and recognition. We accomplish this by having a committed staff of trade show production organizers with the training, technology tools, processes and experience to offer the best service in the industry.
Visit mpassociates.com for more information.

AMS Special Interest Group Event
Addressing Advanced Simulation Challenges from Pure Analog to SoC and IoT Designs

Wednesday, November 4, 2015
5:30 p.m. – 8:00 p.m.
DoubleTree Austin Hotel
Phoenix Central Ballroom

Join us for the free AMS Special Interest Group (SIG) event during ICCAD where our panel of industry-leading experts from semiconductor companies will present their flows and methodologies that address advanced design challenges and enable them to bring products to market more quickly and efficiently.

Agenda
5:30-6:30 p.m.  Welcome Reception
6:30-7:45 p.m.  Dinner and Technical Presentations
7:45-8:00 p.m.  Conclusion and Prize Drawing

Analog/mixed-signal IC designers face challenges at multiple levels that range from device modeling and reliability analysis to complex mixed-signal verification. Synopsys continues to enhance its broad portfolio of circuit simulation solutions to accommodate the higher performance, capacity and complexity required by advanced designs and process technologies.

Attendees will be entered into a drawing to win a GoPro HERO4 Silver camera with accessories!
SUNDAY, NOVEMBER 1

BEST PAPER CANDIDATES & AWARD COMMITTEES

IEEE/ACM William J. McCalla ICCAD Best Paper Award Candidates

Monday, November 2

Session 1A.1: Can’t See the Forest for the Trees: State Restoration’s Limitations in Post-silicon Trace Signal Selection
Sai Ma, Debjit Pal, Rui Jiang - Univ. of Illinois at Urbana-Champaign
Sandip Ray - Intel Corp.
Shobha Vasudevan - Univ. of Illinois at Urbana-Champaign

Tuesday, November 3

Session 4B.2: Defect Clustering-Aware Spare-TSV Allocation for 3D ICs
Shengcheng Wang, Mehdi B. Tahoori - Karlsruhe Institute of Technology
Krishnendu Chakrabarty - Duke Univ.

Session 5A.1: A Polyhedral-based SystemC Modeling and Generation Framework for Effective Low-power Design Space Exploration
Wei Zuo, Warren Kemmerer, Jong Bin Lim - Univ. of Illinois at Urbana-Champaign
Louis-Noël Pouchet - Ohio State Univ.
Andrey Ayupov, Taemin Kim, Kyungtae Han - Intel Corp.
Deming Chen - Univ. of Illinois at Urbana-Champaign

Session 5C.1: DRUM: A Dynamic Range Unbiased Multiplier for Approximate Applications
Soheil Hashemi, R. Iris Bahar, Sherief Reda - Brown Univ.

IEEE/ACM William J. McCalla ICCAD Best Paper Award Selection Committee

Vijaykrishnan Narayanan - Pennsylvania State Univ.
Yu Caio - Arizona State Univ.
Yu Wang - Tsinghua Univ.
Xin Li - Carnegie Mellon Univ.

Ten-Year Retrospective Most Influential Paper Award Selection Committee

Martin Wang - Univ. of Illinois at Urbana-Champaign
Tulika Mitra - National Univ. of Singapore
David Z. Pan - The Univ. of Texas at Austin

ACM SIGDA CADathlon 2015 at ICCAD
Time: 8:00am - 5:00pm | Room: Phoenix South

The CADathlon is a challenging, all-day, programming competition focusing on practical problems at the forefront of Computer-Aided Design, and Electronic Design Automation in particular. The contest emphasizes the knowledge of algorithmic techniques for CAD applications, problem-solving and programming skills, as well as teamwork.

In its fourteenth year as the “Olympic games of EDA,” the contest brings together the best and the brightest of the next generation of CAD professionals. It gives academia and the industry a unique perspective on challenging problems and rising stars, and it also helps attract top graduate students to the EDA field. The contest is open to two-person teams of graduate students specializing in CAD and currently full-time enrolled in a Ph.D. granting institution in any country. Students are selected based on their academic backgrounds and their relevant EDA programming experiences. Travel grants are provided to qualifying students.

The CADathlon competition consists of six problems in the following areas:
(1) Circuit analysis
(2) Physical design
(3) Logic and behavioral synthesis
(4) System design and analysis
(5) Functional verification
(6) Future technologies (Bio-EDA, Security, etc.)

More specific information about the problems and relevant research papers will be released on the Internet one week prior to the competition. The writers and judges that construct and review the problems are experts in EDA from both academia and industry. At the contest, students will be given the problem statements and example test data, but they will not have the judges’ test data. Solutions will be judged on correctness and efficiency. Where appropriate, partial credit might be given. The team that earns the highest score is declared the winner. In addition to handsome trophies, the first and second place teams will receive cash awards. Contest winners will be announced at the ICCAD Opening Session on Monday morning and celebrated at the ACM/SIGDA Dinner and Member Meeting on Tuesday evening.

The CADathlon competition is sponsored by ACM/SIGDA and several Computer and EDA companies, including IBM Research. For detailed contest information and sample problems from last year’s competition, please visit the ACM/ SIGDA website at sigda.org/programs/cadathlon.

Organizing Committee:
Chair: Myung-Chul Kim, mckima@us.ibm.com
Vice Chair: Luis Angel D. Bathen, lbathen@gmail.com
Vice Chair: Jingtong Hu, jthu@okstate.edu
SIGDA Liaison: Yiran Chen, yic52@pitt.edu

Sponsored by:

ACM Association for Computing Machinery
SIGDA
## Monday Schedule

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<td>Opening Session &amp; Awards</td>
<td>Phoenix Central</td>
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<tr>
<td>8:30am - 9:15am</td>
<td>Keynote: Computing for Robots and Biomolecules</td>
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<td>&quot;Lydia E. Kavraki, Rice Univ.&quot;</td>
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<tr>
<td>9:30am - 10:00am</td>
<td>Monday Fast Track Session</td>
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<td>Coffee Break</td>
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<td>Session 1A: Machine Learning in VLSI Design, Yield Estimation and Post-Silicon Validation</td>
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<td>Session 1B: Optimization Techniques for Upcoming Embedded Systems</td>
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<td>Special Session 1C: Self-aware Systems-on-Chip</td>
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<td>Embedded Tutorial 1D: Formal Methods for Emerging Technologies</td>
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<tr>
<td>11:30am - 1:30pm</td>
<td>ACM Student Research Competition Poster Session</td>
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<tr>
<td>12:15pm - 1:15pm</td>
<td>Invited Luncheon Keynote: From Boolean Algebra to Basketball: Applying EDA Techniques to Sports Analytics</td>
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<tr>
<td>1:30pm - 3:30pm</td>
<td>Session 2A: High-Level and Sequential Synthesis</td>
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<td>Session 2B: Keep Austin Wired: Routing and Clocking</td>
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<td>Session 2C: Hardware Based Authentication</td>
<td>Phoenix South</td>
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<td>Special Session 2D: Dennard Scaling is History and Moore's Law is Aging: How to Break the Inevitable Power Wall?</td>
<td>Austin</td>
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<td>3:30pm - 4:00pm</td>
<td>Coffee Break</td>
<td>Prefunction Foyer</td>
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<tr>
<td>4:00pm - 5:30pm</td>
<td>Session 3A: Design Automation for Non-Traditional Architectures</td>
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<td>Session 3B: Modeling, Optimization, and Synthesis of Cyberphysical Systems</td>
<td>Dover's</td>
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<td>Session 3C: The Art of Engineering Heterogeneous Computing Systems</td>
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<td>Special Session 3D: From EDA to DA: Can We Evolve Beyond Our E-Roots?</td>
<td>Austin</td>
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<tr>
<td>5:30pm - 6:00pm</td>
<td>Networking Reception</td>
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<tr>
<td>6:00pm - 6:55pm</td>
<td>Special Session 10A: TAU 2015 Contest on Incremental Timing and CPPR Analysis</td>
<td>Phoenix North</td>
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<tr>
<td>6:00pm - 7:30pm</td>
<td>Special Session 10D: Rebooting Computing and Low Power Image Recognition Challenge</td>
<td>Austin</td>
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<tr>
<td>7:05pm - 8:30pm</td>
<td>Special Session 10B: 2015 CAD Contest</td>
<td>Phoenix North</td>
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- OPENING SESSION & AWARD PRESENTATIONS -

Time: 8:00am - 8:30am | Room: Phoenix Central

Kick off the conference with opening remarks from the ICCAD Executive Committee members and hear the highlights of the conference. The IEEE/ACM William J. McCalla ICCAD Best Paper award will be announced along with other award presentations from IEEE and ACM.

IEEE/ACM William J. McCalla ICCAD Best Paper Award
This award is given in memory of William J. McCalla for his contributions to ICCAD and his CAD technical work throughout his career.

Front-End Award:
Session 5A.1: A Polyhedral-based SystemC Modeling and Generation Framework for Effective Low-power Design Space Exploration
Wei Zuo, Warren Kemmerer, Jong Bin Lim - Univ. of Illinois at Urbana-Champaign
Louis-Noël Pouchet - Ohio State Univ.
Andrey Ayupov, Taemin Kim, Kyungtae Han - Intel Corp.
Deming Chen - Univ. of Illinois at Urbana-Champaign

Back-End Award:
Session 4B.2: Defect Clustering-Aware Spare-TSV Allocation for 3D ICs
Shengcheng Wang, Mehdi Tahoori - Karlsruhe Institute of Technology
Krishnendu Chakrabarty - Duke Univ.

Ten Year Retrospective Most Influential Paper Award
This award is being given to the paper judged to be the most influential on research and industrial practice in computer-aided design over the ten years since its original appearance at ICCAD.

2005 Paper Titled: Performance Analysis of Carbon Nanotube Interconnects for VLSI Applications
Navin Srivastava, Kaustav Banerjee - Univ. of California, Santa Barbara
ICCAD 2005, pp. 383 – 390
Computing for Robots and Biomolecules

Lydia E. Kavraki - Rice Univ.

Time: 8:30am - 9:15am | Room: Phoenix Central

Over the last decade, the development of fast and reliable motion planning algorithms has deeply influenced many domains in robotics, such as industrial automation and autonomous exploration. Motion planning has also contributed to great advances in an array of unlikely fields, including graphics animation and computational structural biology.

This talk will first describe how sampling-based methods revolutionized motion planning in robotics. The presentation will quickly focus on recent algorithms that are particularly suitable for systems with complex dynamics. The talk will then introduce an integrative framework that allows the synthesis of motion plans from high-level specifications. The framework uses temporal logic and formal methods and establishes a tight link between classical motion planning in robotics and task planning in artificial intelligence. Although research initially began in the realm of robotics, the experience gained has led to algorithmic advances for analyzing the motion and function of proteins, the worker molecules of all cells. This talk will conclude by discussing robotics-inspired methods for computing the flexibility of proteins and large macromolecular complexes with the ultimate goals of deciphering molecular function and aiding the discovery of new therapeutics.

Biography:
Lydia E. Kavraki is the Noah Harding Professor of Computer Science and Professor of Bioengineering at Rice University. She received her B.A. in Computer Science from the University of Crete in Greece and her Ph.D. from Stanford University. Her research focuses on physical algorithms and their applications in robotics, computational structural biology, and translational bioinformatics.

Kavraki has authored more than 200 peer-reviewed journal and conference publications and is one of the authors of the widely-used robotics textbook titled "Principles of Robot Motion" published by MIT Press. Kavraki currently serves as an associate editor for several journals including the International Journal of Robotics Research, the ACM/IEEE Transactions on Computational Biology and Bioinformatics, Frontiers in Molecular Biosciences, and Springer Tracts in Advanced Robotics. She is the recipient of the 2000 Association for Computing Machinery (ACM) Grace Murray Hopper Award, a Fellow of ACM, IEEE, AAAS, AAAI, AIMBE, and a member of the National Academy of Medicine.
1B - Optimization Techniques for Upcoming Embedded Systems

*Time: 10:30am - 12:00pm | Room: Dover’s*

**Moderator:**
Andreas Gerstlauer - Univ. of Texas at Austin

This session addresses new challenges posed by emerging memory technologies, and runtime reconfigurable solutions.

The first paper in the session focuses on a light-weight controller for PCM-based main memory technologies that exploit TLB miss information. The second paper proposes reshaping of access patterns for embedded multi-media controllers for solid-state drives. The third paper proposes a stress-aware placement technique to mitigate aging for reconfigurable architectures.

1B.1 A Light-Weighted Software-Controlled Cache for PCM-based Main Memory Systems
Hung-Sheng Chang - National Taiwan Univ.
Yuan-Hao Chang - Academia Sinica
Tei-Wei Kuo - Academia Sinica & National Taiwan Univ.
Hsiang-Pang Li - Macronix International Co., Ltd.

1B.2 Access Pattern Reshaping for eMMC-enabled SSDs
Chien-Chung Ho - National Taiwan Univ.
Yuan-Hao Chang - Academia Sinica
Tei-Wei Kuo - Academia Sinica & National Taiwan Univ.

1B.3 STRAP: Stress-Aware Placement for Aging Mitigation in Runtime Reconfigurable Architectures
Hongyan Zhang - Karlsruhe Institute of Technology
Michael A. Kochte, Eric Schneider - Univ. of Stuttgart
Lars Bauer - Karlsruhe Institute of Technology
Hans-Joachim Wunderlich - Univ. of Stuttgart
Jörg Henkel - Karlsruhe Institute of Technology

Special Session 1C - Self-aware Systems-on-Chip

*Time: 10:30am - 12:00pm | Room: Phoenix South*

**Moderator:**
Ulf Schlichtmann - Technische Univ. München

**Organizer:**
Mehdi B. Tahoori - Karlsruhe Institute of Technology

While the notion of self-awareness has a long history in biology, psychology, medicine, engineering and (more recently) computing, we are seeing the emerging need for self-awareness in the context of complex many-core Systems-on-Chip that must address the often conflicting requirements of performance, resiliency, energy, heat, cost, security, etc. in the face of highly dynamic operational behaviors coupled with process, environment, and workload variabilities. Unlike traditional MultiProcessor Systems-on-Chip (MPSoCs), self-aware SoCs must deploy an intelligent co-design of the control, communication, and computing infrastructure that interacts with the physical environment in real-time in order to modify the system’s behavior so as to adaptively achieve desired objectives and Quality-of-Service (QoS). Self-aware SoCs require a combination of ubiquitous sensing and actuation, health-monitoring, and statistical model-building to enable the SoC’s adaptation over time and space. Accordingly, this special session first outlines the notions of self-awareness in computing and then features three different dimensions of self-aware Systems-on-Chip.

The first talk by Prof. Nikil Dutt defines the notion of self-aware computing and presents the Cyber-Physical System-on-Chip (CPSoC) concept as an exemplar of a self-aware SoC that intrinsically couples on-chip and cross-layer sensing and actuation using a sensor-actuator rich fabric to enable self-awareness. The second talk by Prof. Mehdi Tahoori discusses data-driven learning based chip health monitoring infrastructure to ensure system resilience. The third talk by Prof. Abhijit Chatterjee presents self-aware self-learning real-time systems with applications to wireless communication, signal processing and control.

1C.1 Self-Aware Cyber-Physical Systems-on-Chip
Nikil Dutt - Univ. of California, Irvine
Axel Jantsch - Technische Univ. Wien
Santanu Sarma - Univ. of California, Irvine

1C.2 Fine-Grained Aging Prediction Based on the Monitoring of Run-Time Stress Using DfT Infrastructure
Abhishek Koneru - Duke Univ.
Arunkumar Vijayan - Karlsruhe Institute of Technology
Krishnendu Chakrabarty - Duke Univ.
Mehdi B. Tahoori - Karlsruhe Institute of Technology

1C.3 Self Learning Analog/Mixed-Signal/RF Systems: Dynamic Adaptation to Workload and Environmental Uncertainties
Debashis Banerjee, Shreyas Sen, Abhijit Chatterjee - Georgia Institute of Technology
Embedded Tutorial 1D - Formal Methods for Emerging Technologies

**Time:** 10:30am - 12:00pm | **Room:** Austin

**Moderator:**
Rolf Drechsler - Univ. of Bremen & DFKI GmbH

**Organizer:**
Robert Wille - Univ. of Bremen & DFKI GmbH

Formal Methods advanced to an important core technology in Computer-Aided Design (CAD). At the same time, researchers and engineers also started the investigation of so-called emerging technologies such as quantum computation, reversible computation, optical circuits, or biochips. Although most of these technologies are still in a rather "academic" state, first physical realizations have already been presented or even entered the market recently. This motivates a more detailed consideration of how to design circuits for these technologies. As for conventional circuits, formal methods do play an important role here.

In this tutorial, we are aiming to address the current momentum caused by the recent accomplishments and provide a comprehensive introduction into these emerging technologies as well as their corresponding CAD methods. This will include a special focus on how formal methods may help in the design and verification of circuits for those technologies.

1D.1 Formal Methods for Emerging Technologies
Robert Wille - Univ. of Bremen & DFKI GmbH
Rolf Drechsler - Univ. of Bremen & DFKI GmbH

ACM Student Research Competition Poster Session

**Time:** 11:30am - 1:30pm | **Room:** DeZavala

**Organizers:**
Tsung-Yi Ho - National Tsing Hua Univ.
Yiyu Shi - Univ. of Notre Dame

Sponsored by Microsoft Research, the ACM Student Research Competition (SRC) is an internationally recognized venue enabling undergraduate and graduate students who are members of ACM and ACM SIGDA to:

- Experience the research world—for many undergraduates this is a first!
- Share research results and exchange ideas with other students, judges, and conference attendees.
- Rub shoulders with academic and industry luminaries.
- Understand the practical applications of their research.
- Perfect their communication skills.
- Receive prizes and gain recognition from ACM, and the greater computing community.

ACM SRC has three rounds:
(1) Abstract review
(2) Poster session (this session)
(3) Technical presentation

In the first round, 2-page research abstracts are evaluated by EDA experts from academia and industry to select participants for the second round (this session). For the ACM SRC at ICCAD 2015 competition, 20 participants were invited to present their research at ICCAD. The posters are evaluated by EDA experts to select 5 participants in graduate and undergraduate categories to advance to the final round (technical presentation round). Students are expected to discuss their work with judges. Each judge will rate the student’s visual presentation based on the criteria of uniqueness of the approach, the significance of the contribution, visual presentation, and quality of presentation.

More details can be found at sigda.org/src.
From Boolean Algebra to Basketball: Applying EDA Techniques to Sports Analytics

Charles J. Alpert - Cadence Design Systems, Inc.

Time: 12:15pm - 1:15pm | Room: Phoenix Central

Professional sports are big business. The National Football League generates over ten billion dollars annually, but this is actually less than fantasy sports, which generates 15 billion in revenue (about double the entire EDA industry). Not surprisingly, the interest in utilizing data analytics for sports applications has exploded in recent years. The algorithm techniques utilized share significant overlap with traditional EDA algorithms. Win and playoff prediction tools utilize Monte Carlo simulation. Similar to how model-order reduction can produce simplified circuits, analytic techniques aggregate mountains of player statistics to model the a player's actual value.

In this talk, we describe how EDA techniques can be applied to college basketball, or more specifically, the NCAA tournament.

Each March, the NCAA tournament pits 64 of the best college basketball teams into a single elimination tournament to determine the national champion. The first round has 32 matches, the second round has 16 matches, and so on, until a single champion emerges. Millions of fans, including President Obama, participate in "bracketology" pools in which they predict the winners for each of these 63 matches. Millions of participants enter their picks on sports media websites hoping to earn office bragging rights or to win major prizes. Once the tournament starts, automatic software tracks contestants' correct picks, their maximum score, and their current place in the standings. However, today's websites lack sufficient information to show participants how they are performing. This talk shows how simulation can be used to determine each participants probability of winning. We also discuss how logic synthesis can be applied to determine the exact winning scenarios for each participant. Finally, the talk will present other sports problems which are suitable for algorithmic innovation.

Biography:
Charles (Chuck) Alpert joined Cadence Design Systems in 2014, where he serves as a Group Director for the Digital Signoff Group. His team researches and develops next generation algorithms, solutions, and methodologies for Cadence's digital implementation tools. Prior to that, Chuck spent 17 years working for the IBM Research Division, developing internal EDA tools in the physical design space. He received a Ph.D. in Computer Science from UCLA in 1996 and a B.S. and a B.A. degree from Stanford in 1991. Chuck's interests include algorithms for placement, routing, wire synthesis, clocking and for sports analysis. He is an IEEE Fellow and has published over 100 conference and journal publications and has filed 100 patents. He currently serves as Deputy Editor-in-Chief for IEEE Transactions on CAD. Chuck chaired the ISPD and Tau conferences and is serving as general chair for DAC 2016 in Austin.

2A - High-Level and Sequential Synthesis

Time: 1:30pm - 3:30pm | Room: Phoenix North

Moderator:
Flavio M. de Paula - IBM Corp.

In this session, the first three papers present advances in scheduling, acceleration, and architecture of high-level synthesis (HLS) systems. The session starts with an approach that exploits code transformation to improve HLS performance. The second paper uses an accelerator for parallelizing loops in hardware. The third contribution introduces a new "buslet" architecture to improve wire-ability of a HLS design. In the last paper, we take a new look at the state minimization problem for Mealy machines, using a Satisfiability formulation.

2A.1 Code Transformations Based on Speculative SDC Scheduling
Marco Lattuada, Fabrizio Ferrandi - Politecnico di Milano

2A.2 ElasticFlow: A Complexity-Effective Approach for Pipelining Irregular Loop Nests
Mingxing Tan - Cornell Univ. & Google, Inc.
Gai Liu, Ritchie Zhao, Steve Dai, Zhiru Zhang - Cornell Univ.

2A.3 Communication Scheduling and Buslet Synthesis for Low-Interconnect HLS Designs
Enzo Tartaglione, Shantanu Dutt - Univ. of Illinois at Chicago

2A.4 MeMin: SAT-based Exact Minimization of Incompletely Specified Mealy Machines
Andreas Abel, Jan Reineke - Saarland Univ.
2B - Keep Austin Wired: Routing and Clocking

*Time: 1:30pm - 3:30pm | Room: Dover's*

**Moderator:**
Jia Wang - Illinois Institute of Technology

Keeping Austin Wired is easy! But keeping modern VLSI chips wired with performance and power budgets is hard. In this session, new efforts for wiring chips will be presented. The first paper presents a framework that handles the performance constraints in global routing. The second one discusses how to improve performance by layer re-assignment. The third paper proposes parallel algorithms to speed up FPGA routing. The final paper presents a technique to synthesize clock spines for high performance designs.

2B.1 **Global Routing with Inherent Static Timing Constraints**
Stephan Held, Dirk Müller, Daniel Rotter, Vera Traub, Jens Vygen - Univ. of Bonn

2B.2 **TILA: Timing-Driven Incremental Layer Assignment**
Bei Yu - Chinese Univ. of Hong Kong
Derong Liu - Univ. of Texas at Austin
Salim Chowdhury - Oracle Corporation
David Z. Pan - Univ. of Texas at Austin

2B.3 **Accelerate FPGA Routing with Parallel Recursive Partitioning**
Minghua Shen, Guojie Luo - Peking Univ.

2B.4 **Synthesis for Power-Aware Clock Spines**
Hyungjung Seo - Samsung Electronics Co., Ltd.
Juyeon Kim - Seoul National Univ.
Minseok Kang - Samsung Electronics Co., Ltd.
Taewhan Kim - Seoul National Univ.

2C - Hardware Based Authentication

*Time: 1:30pm - 3:30pm | Room: Phoenix South*

**Moderator:**
Bao Liu - Univ. of Texas at San Antonio

This session presents novel techniques for hardware authentication. Specifically, Paper 1 replaces ECC, typically used along PUFs for authentication, with a novel fault tolerance algorithm based on ring weights. Paper 2 exploits the unique features of emerging resistive RAM technology for user password authentication. Paper 3 presents an on-chip aging sensor based on electromigration to detect recycled ICs. Finally, Paper 4 embeds capacitors in the internal layer of a printed circuit board in order to verify its authenticity.

2C.1 **A Novel Way to Authenticate Untrusted Integrated Circuits**
Wei Yan, John Chandy, Fatemeh Tehranipoor - Univ. of Connecticut

2C.2 **RRAM Based Lightweight User Authentication**
Md Tanvir Arafin, Gang Qu - Univ. of Maryland

2C.3 **EM-Based on-Chip Aging Sensor for Detection and Prevention of Counterfeit and Recycled ICs**
Kai He, Xin Huang, Sheldon X.-D. Tan - Univ. of California, Riverside

2C.4 **BoardPUF: Physical Unclonable Functions for Printed Circuit Board Authentication**
Lingxiao Wei, Chaosheng Song, Yannan Liu, Jie Zhang, Feng Yuan, Qiang Xu - Chinese Univ. of Hong Kong
Special Session 2D - Dennard Scaling is History and Moore’s Law is Aging: How to Break the Inevitable Power Wall?

**Time:** 1:30pm - 3:30pm | **Room:** Austin

**Moderator:**
Sachin S. Sapatnekar - Univ. of Minnesota

**Organizer:**
Paul Bogdan - Univ. of Southern California

The relentless increase in integration densities is paving the way for full system on-chip integration and widespread adoption of multi-/manycore chips in several application domains. From consumer multimedia to high-end applications (security, healthcare, big data, etc.), new designs containing a large number of embedded cores are emerging, but potential showstoppers include challenges related to power/energy and thermal efficiencies. For a dependable manycore system, power/energy efficiency is of utmost concern due to cost, performance, scalability, and environmental impact. Moreover, increased power densities can raise on-chip temperatures, which in turn can decrease chip reliability and performance, and increase cooling costs.

Given the current trends in terms of power and performance, it is not practical to follow existing methodologies to design tomorrow’s thousand-core platforms. Consequently, new, out-of-the-box approaches need to be explored. In this special session, we will describe new, far-reaching power-efficient techniques that achieve the most sought after feature in massively integrated single-chip manycore computing platforms.

2D.1 Fine-Grain Power Management in Manycore Processor and System-on-Chip (SoC) Designs
Vivek De - Intel Corp.

2D.2 The (Low) Power of Less Wiring: Enabling Energy Efficiency in Many-Core Platforms Through Wireless NoC
Partha Pande, Ryan Gary Kim - Washington State Univ.
Zhao Chen - Carnegie Mellon Univ.
Wonje Choi - Washington State Univ.
Diana Marculescu, Radu Marculescu - Carnegie Mellon Univ.

Paul Bogdan, Yuankun Xue - Univ. of Southern California

2D.4 Mitigating the Power Density and Temperature Problems in the Nano-Era
Muhammad Shafique, Jörg Henkel - Karlsruhe Institute of Technology

2D.5 Power and Microarchitecture Tradeoffs in Next-Generation Manycores: From Homogeneous to Heterogeneous Cores and Everything in Between
Partha Kundu - Broadcom Corp.

3A - Design Automation for Non-Traditional Architectures

**Time:** 4:00pm - 5:30pm | **Room:** Phoenix North

**Moderator:**
Iris Bahar - Brown Univ.

Non-traditional design and architecture have been widely explored for smaller density, higher speed and lower energy consumption. Challenges for non-traditional architecture and new CAD methodologies will be presented in this session. It starts with a stochastic circuit optimization methodology for accuracy and energy tradeoffs. The second presentation talks about an analytic model to estimate the power and performance of cellular neural network. A case study is conducted to compare the CNN design based on emerging non-linear TFET solution and conventional linear resistor based design. In the last paper, the non-ideal synaptic device characteristics and the impact on on-chip learning will be studied.

3A.1 Optimizing Stochastic Circuits for Accuracy-Energy Tradeoffs
Armin Alaghi - Univ. of Michigan
Wei-Ting J. Chan - Univ. of California at San Diego
John P. Hayes - Univ. of Michigan
Andrew B. Kahng, Jiajia Li - Univ. of California at San Diego

3A.2 Analytically Modeling Power and Performance of a CNN System
Indranil Palit, Qiuwen Lou, Nicholas Acampora, Joseph Nahas, Michael Niemier, X. Sharon Hu - Univ. of Notre Dame

3A.3 Mitigating Effects of Non-ideal Synaptic Device Characteristics for On-chip Learning
Pai-Yu Chen - Arizona State Univ.
Binbin Lin - Univ. of Michigan
I-Ting Wang, Tuo-Hung Hou - National Chiao Tung Univ.
Jieping Ye - Univ. of Michigan
Sarma Vrudhula, Jae-sun Seo, Yu Cao, Shimeng Yu - Arizona State Univ.
3B - Modeling, Optimization, and Synthesis of Cyberphysical Systems

Time: 4:00pm - 5:30pm | Room: Dover's

Moderator:
Eli Bozorgzadeh - Univ. of California, Irvine

This session introduces design frameworks that address modeling, optimization, and synthesis of cyberphysical systems. The target applications include wearable brain machine interface, chance-constrained control systems, and aircraft environment control systems. The first paper presents methodologies for synthesizing wearable brain-machine interface. The second paper introduces an approach for chance-constrained optimization through simulations. The third paper introduces discrete-continuous optimization for cyberphysical system architecture exploration.

3B.1 Robust Communication with IoT Devices using Wearable Brain Machine Interfaces
Md Muztoba, Ujjwal Gupta, Tanvir Mustofa, Umit Y. Ogras - Arizona State Univ.

3B.2 Simulation-Guided Parameter Synthesis for Chance-Constrained Optimization of Control Systems
Yan Zhang - National Univ. of Singapore
Sriram Sankaranarayanan - Univ. of Colorado
Benjamin Gyori - Harvard Univ.

3B.3 A Mixed Discrete-Continuous Optimization Scheme for Cyber-Physical System Architecture Exploration
John Finn, Pierluigi Nuzzo, Alberto Sangiovanni-Vincentelli - Univ. of California, Berkeley

3C - The Art of Engineering Heterogeneous Computing Systems

Time: 4:00pm - 5:30pm | Room: Phoenix South

Moderator:
Peter Hofstee - IBM Research - Austin

Heterogeneous computing promises to be a means for more efficient computing. By leveraging the best characteristics of different compute mediums such as CPUs, GPUs, and FPGAS, it enables the exploration of multiple design goals, such as low energy consumption, high performance, etc. In this session, we will examine three exciting application spaces which have successfully been accelerated by exploiting various heterogeneous approaches.

3C.1 A User-Centric CPU-GPU Governing Framework for 3D Games on Mobile Devices
Wei-Ming Chen, Sheng-Wei Cheng - National Taiwan Univ.
Pi-Cheng Hsiu - Academia Sinica
Tei-Wei Kuo - Academia Sinica & National Taiwan Univ.

3C.2 SAT Solving using FPGA-based Heterogeneous Computing
Jason Thong, Nicola Nicolici - McMaster Univ.

3C.3 Heterogeneous Hardware/Software Acceleration of the BWA-MEM DNA Alignment Algorithm
Nauman Ahmed - Delft Univ. of Technology
Vlad-Mihai Sima, Ernst Houtgast - Bluebee
Koen Bertels, Zaid Al-Ars - Delft Univ. of Technology
Special Session 3D - From EDA to DA: Can We Evolve Beyond Our E-Roots?

**Time:** 4:00pm - 5:30pm | **Room:** Austin

**Moderator:**
 Deming Chen - Univ. of Illinois at Urbana-Champaign

**Organizers:**
 Andrew B. Kahng - Univ. of California at San Diego
 Farinaz Koushanfar - Rice Univ.

As we approach a 2020 "wall" of silicon, patterning, device, interconnect and cost limits, and as EDA technologies and the industry itself remain in their present "mature" state, it is now more urgent to revisit question of how the field will evolve and grow. In particular, how can the paradigms and research methodologies of EDA be leveraged for design automation (DA) in other, emerging domains? Some researchers in our community are actively contributing to DA for a variety of other fields (e.g., emerging nanotechnologies, biomedical and security).

But, evolution and growth as a community requires a much more systematic, coherent effort - as well as forward-looking vision to steer by. This special session is built upon and follows up on the seeds planted by the CCC Extreme Scale Design Automation workshop series. It focuses on recent efforts to systematize knowledge, trends, metrics, and visions that can help enable the EDA community to move beyond its E-roots. The audience will learn about a new IEEE CEDA technical activity group dedicated to this subject. The session includes four 15-minute talks, covering the overview and study teams within the technical activity group, as well as a 30-minute panel summarizing the recent DA challenge at DAC'15.

**PANEL: DA Perspective Challenge @DAC’15: Summary and Vision**

Panelists:
- Steven P. Levitan - Univ. of Pittsburgh
- Sani Nassif - Radyalis, LLC
- Naehyuck Chang - KAIST
- Jim Huang - HP Labs
- Yiran Chen - Univ. of Pittsburgh

3D.1 Evolving EDA Beyond its E-Roots: An Overview
Andrew B. Kahng - Univ. of California at San Diego
Farinaz Koushanfar - Rice Univ.

3D.2 DA Systemization of Knowledge: A Catalog of Prior Forward-Looking Initiatives
Farinaz Koushanfar, Azalia Mirhoseini - Rice Univ.
Gang Qu - Univ. of Maryland
Zhiru Zhang - Cornell Univ.

3D.3 Toward Metrics of Design Automation Research Impact
Andrew B. Kahng - Univ. of California at San Diego
Mulong Luo - Univ. of California at San Diego
Gi-Joon Nam - IBM Research
Siddhartha Nath - Univ. of California at San Diego
David Z. Pan - Univ. of Texas at Austin
Gabriel Robins - Univ. of Virginia

3D.4 DA Vision 2015: From Here to Eternity
Miodrag Potkonjak - Univ. of California, Los Angeles
Deming Chen - Univ. of Illinois
Priyank Kalla - Univ. of Utah
Steven P. Levitan - Univ. of Pittsburgh

Networking Reception

**Time:** 5:30pm - 6:00pm | **Room:** Prefunction Foyer

Whatever your goal, Networking Receptions are the perfect venue for you to expand your network and keep you connected! Join us today to catch up with your colleagues and discuss the day’s presentations with the conference presenters. The reception is included with your conference registration fee.

Special Session 10A - TAU 2015 Contest on Incremental Timing and CPPR Analysis

**Time:** 6:00pm - 6:55pm | **Room:** Phoenix North

**Moderator:**
Jin Hu - IBM Corp.

**Organizers:**
Jin Hu - IBM Corp.
Greg Schaeffer - IBM Corp.
Vibhor Garg - Cadence Design Systems, Inc.

Among timing analysis applications, timing-driven operations are imperative for the success of optimization flows, such as placement, routing, logic synthesis, and physical synthesis. Optimization transforms change the design, and therefore have the potential to significantly affect timing information. As such, timing must be kept current to ensure slack integrity and timing closure. For reasonable turnaround and performance, the timer should only incrementally update the affected portion of the design.

The aim of the TAU 2015 Contest on Incremental Timing and CPPR Analysis is to seek novel ideas for incremental timing analysis by: (i) introducing the concept and motivating the importance of incremental timing analysis and incremental common path pessimism removal (CPPR), (ii) encourage novel parallelization techniques (including multi-threading), and (iii) facilitating the creation of an incremental timing analysis framework with benchmarks to further advance this research area. This session highlights the ideas and practices of the top-performing teams of the TAU 2015 Contest.

10A.1 TAU 2015 Contest on Incremental Timing Analysis
Jin Hu, Greg Schaeffer - IBM Corp.
Vibhor Garg - Cadence Design Systems, Inc.

10A.2 iTimerC 2.0: Fast Incremental Timing and CPPR Analysis

10A.3 OpenTimer: A High-Performance Timing Analysis Tool
Tsung-Wei Huang, Martin D. F. Wong - Univ. of Illinois at Urbana-Champaign

10A.4 iitRACE: A Memory Efficient Engine for Fast Incremental Timing Analysis and Clock Pessimism Removal
Chaitanya Peddawad, Aman Goel, Dheeraj B, Nitin Chandrachoodan - Indian Institute of Technology Madras

All speakers are denoted in bold | * denotes Best Paper Candidate
Special Session 10D - Rebooting Computing and Low Power Image Recognition Challenge

*Time: 6:00pm - 7:30pm | Room: Austin*

**Moderator:**
Yung-Hsiang Lu - Purdue Univ.

**Organizer:**
Yung-Hsiang Lu - Purdue Univ.

“Rebooting Computing” (RC) is an effort in the IEEE to rethink future research of computers. RC started in 2012 by the co-chairs, Elie Track (IEEE Council on Superconductivity) and Tom Conte (Computer Society). RC takes a holistic approach, considering revolutionary as well as evolutionary solutions needed to advance computer technologies. Three summits have been held in 2013 and 2014, discussing different technologies, from emerging devices to user interface, from security to energy efficiency, from neuromorphic to reversible computing. The first part of this special session introduces RC to the CAD community and solicits revolutionary ideas from the community for the directions of future computer research.

Energy efficiency is identified as one of the most important challenges in future computer technologies. The importance of energy efficiency spans from miniature embedded sensors to wearable computers, from individual desktops to mega-Watt data centers. To gauge the state of the art, the RC Committee organized the first Low Power Image Recognition Challenge (LPIRC) on June 7, 2015 in San Francisco. Each image contains one or multiple objects, among 200 categories. A participant has to provide a system that can recognize the objects and report the bounding boxes of the objects. The second part of this special session explains LPIRC and the top two winners will present their solutions.

10D.1 Rebooting Computing
Thomas M. Conte - IEEE & Georgia Institute of Technology
Erik P. DeBenedictis - Sandia National Laboratories
Bichlien Hoang - IEEE
Alan M. Kadin - Princeton Junction
Yung-Hsiang Lu - Purdue Univ.
Elie K. Track - nVizix LLC & IEEE

10D.2 Low Power Image Recognition Challenge
Alexander C. Berg - Univ. of North Carolina, Chapel Hill
Rachit Garg - Purdue Univ.
Ganesh Gingade - Hughes Network Systems, LLC & Purdue Univ.
Wei Liu - Univ. of North Carolina, Chapel Hill
Yung-Hsiang Lu - Purdue Univ.

10D.3 Pipelined Fast RCNN on Embedded GPU
Boxun Li, Huizi Mao, Tianqi Tang, Yu Wang - Tsinghua Univ.
Jun Yao - Huawei Technologies Co., Ltd.

10D.4 Object Detection Based on Fast Object Proposal and Representation
Yongzhen Huang, Jingyu Liu, Junran Peng, Jingqiu Wang - Institute of Automation, Chinese Academy of Sciences
Tao Wang, Jun Yao - Huawei Technologies Co., Ltd.

Special Session 10B - 2015 CAD Contest

*Time: 7:05pm - 8:30pm | Room: Phoenix North*

**Moderators:**
Natarajan Viswanathan - IBM Corp.
Shih-Hsu Huang - Chung Yuan Christian Univ.

**Organizer:**
Natarajan Viswanathan - IBM Corp.

The CAD contests at ICCAD and associated benchmark suites have been instrumental in advancing the state-of-the-art in EDA. Additionally, they have fostered productive industry-academia collaboration. In its fourth year, the 2015 CAD contest is among the largest worldwide EDA contests, attracting 112 teams from 12 regions/countries. This year’s contest is a challenging, multi-month, research and development competition, focusing on advanced, real-world problems in the three areas of system level design, logic synthesis & verification, and physical design.

This special session presents the three contest problems, releases the associated benchmarks, and announces the winners. The session also provides a venue for the top-performing teams to showcase their key ideas via short video presentations.

10B.1 Overview of the 2015 CAD contest at ICCAD
Natarajan Viswanathan - IBM Corp.
Shih-Hsu Huang - Chung Yuan Christian Univ.
Rung-Bin Lin - Yuan Ze Univ.
Myung-Chul Kim - IBM Corp.

10B.2 ICCAD 2015 Contest in 3D Interlayer Cooling Optimized Network
Arvind Sridhar - IBM Research - Zurich
Mohamed M. Sabry - Stanford Univ.
David Atienza - École Polytechnique Fédérale de Lausanne

10B.3 ICCAD-2015 CAD Contest in Large-scale Equivalence Checking and Function Correction and Benchmark Suite
Chih-Jen Hsu, Chi-An Wu - Cadence Taiwan, Inc.
Wei-Hsun Lin, Kei-Yong Khoo - Cadence Design Systems, Inc.

10B.4 ICCAD-2015 CAD Contest in Incremental Timing-driven Placement and Benchmark Suite
Myung-Chul Kim - IBM Corp.
Jin Hu - IBM Corp.
Jiajia Li - Univ. of California at San Diego
Natarajan Viswanathan - IBM Corp.

**Sponsored by:**

[cadence](#)
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<td>Session 5A: Simulation for Parallel and Accelerated Computing</td>
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<td>4:00pm - 6:00pm</td>
<td>Session 6A: New CAD Directions for Emerging Technologies</td>
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<td>Session 6B: Modern-Day Placement</td>
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<td>12:10pm - 1:20pm</td>
<td>Invited Luncheon Keynote: The Future of Energy-Efficient Computing</td>
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<td>Dr. Stephen W. Keckler, NVIDIA Corporation</td>
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<td>6:00pm - 6:30pm</td>
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<tr>
<td>6:30pm - 8:00pm</td>
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ACM Student Research Competition Technical Presentations

**Time:** 8:00am - 10:00am | **Room:** Phoenix South

**Organizers:**
- Tsung-Yi Ho - National Tsing Hua Univ.
- Yiyu Shi - Univ. of Notre Dame

The ACM Student Research Competition allows both graduate and undergraduate students to discuss their research with student peers, as well as academic and industry researchers, in an informal setting, while enabling them to attend ICCAD.

This session is the final round of ACM SRC at ICCAD 2015. Each student will present for 10 minutes, followed by a 5-minute question and answer period. This session will be attended by the evaluators and any interested conference attendees. The top three winners in each category will be chosen based on these presentations.

The undergraduate and graduate finalists will be eligible to compete in the ACM SRC Grand Finals to be held in June 2016. More details can be found at sigda.org/src.

**Tuesday Fast Track Session**

**Time:** 9:30am - 10:00am | **Room:** Phoenix Central

Get on the Fast Track to Tuesday with a 45-second preview of upcoming presentations for the day.

4A - Reliability Goes Vertical

**Time:** 10:30am - 12:00pm | **Room:** Phoenix North

**Moderator:**
Raju Balasubramanian - IBM Corp.

This session includes new approaches for design flows from software, processor to circuit components. The first paper proposes to use loop transformation to improve software reliability. The second paper applies formal specifications to design reliable processors. The last paper focuses on error analysis for multipliers.

4A.1 Impact of Loop Transformations on Software Reliability
Jason Cong, Cody Hao Yu - Univ. of California, Los Angeles

4A.2 Error-Tolerant Processors: Formal Specification and Verification
Ameneh Golnari, Yakir Vizel, Sharad Malik - Princeton Univ.

4A.3 FEMTO: Fast Error Analysis in Multipliers through Topological Traversal
Deepashree Sengupta, Sachin S. Sapatnekar - Univ. of Minnesota

4B - Advancements in Adaptive Test, 3D-IC Yield Improvement, and Silicon Debug

**Time:** 10:30am - 12:00pm | **Room:** Dover’s

**Moderator:**
Hank Walker - Texas A&M Univ.

This session covers advancements in three important IC testing topics. In the first paper, a proximity-based adaptive test technique is proposed to improve test quality by test escape screening. The second paper discusses spare TSV allocation for 3D-IC yield improvement considering defect clustering and TSV stress induced delay. The last paper investigates the capability of a software-based silicon debug technique in localizing power supply noise induced timing failures.

4B.1 Pairwise Proximity-Based Features for Test Escape Screening
Fan Lin, Chun-Kai Hsu, Alberto G. Busetto, Kwang-Ting (Tim) Cheng - Univ. of California, Santa Barbara

*4B.2 Defect Clustering-Aware Spare-TSV Allocation for 3D ICs
Shengcheng Wang, Mehdi B. Tahoori - Karlsruhe Institute of Technology
Krishnendu Chakrabarty - Duke Univ.

Yutaka Masuda, Masanori Hashimoto, Takao Onoye - Osaka Univ.

Sponsored by:
Special Session 4C - Accelerators for High Performance Data Analytics

**Time:** 10:30am - 12:00pm | **Room:** Phoenix South

**Moderator:**
Steve Wallach - Micron Technology, Inc.

**Organizers:**
Antonino Tumeo - Pacific Northwest National Lab
Vito Giovanni Castellana - Pacific Northwest National Lab

Emerging data analytics applications are experiencing an exponential growth in the availability of data. Extracting value from the data poses operational challenges not only for their size, but also for reaching the performance required to provide actionable results under variable deadlines. A space efficient way to organize these data is using pointer- or linked-list based data structures such as graphs. Graphs expose a significant amount of inherent task level parallelism, but they also generate unpredictable, fine-grained, data accesses. Furthermore, graph algorithms usually are synchronization intensive and mainly memory bandwidth bound. In summary, they induce an irregular behavior.

Custom accelerators are emerging as a promising solution to accelerate data-intensive workloads. Several new architectures based on reconfigurable devices have recently appeared. These include: the Convey Wolverine coprocessors, the Microsoft Bing accelerator, and various custom accelerators for graph-based applications. Nevertheless, there still are significant gaps between the complexity and variety of these workloads, and the applicability of custom accelerators. These ultimately reside in the design tools, which should provide a fast and flexible path from high-level specifications to efficient Register-Transfer Level code. Historically, tools have targeted regular, arithmetic intensive workloads, mainly exposing instruction level parallelism, but they also generate unpredictable, fine-grained, data accesses. Furthermore, graph algorithms usually are synchronization intensive and mainly memory bandwidth bound. In summary, they induce an irregular behavior.

This special session presents three talks that discuss how current solutions in terms of architectures, design methodologies, and tools address these challenges, identify potentials for improvements, and provide research directions.

4C.1 **High Level Synthesis of RDF Queries for Graph Analytics**
Vito Giovanni Castellana, Marco Minutoli - Pacific Northwest National Lab
Marco Lattuada - Politecnico di Milano
Alessandro Morari, Antonino Tumeo - Pacific Northwest National Lab
Fabrizio Ferrandi - Politecnico di Milano

4C.2 **Enabling Programmers and Compilers to Efficiently Target Reconfigurable Architectures with the Hybrid Threading Approach**
Glen Edwards - Micron Technology, Inc.

4C.3 **CAMs as Synchronizing Caches for Multithreaded Irregular Applications on FPGAs**
Skyler Windh, Prerna Budhkar, Walid A. Najjar - Univ. of California, Riverside

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Special Session 4D - Hardware Authentication: From ICs to IoTs

**Time:** 10:30am - 12:00pm | **Room:** Austin

**Moderator:**
Swarup Bhunia - Univ. of Florida

**Organizer:**
Swarup Bhunia - Univ. of Florida

Embedded computing devices today contain large amounts of sensitive assets (e.g. cryptographic keys, premium content, and firmware), which must be protected from unauthorized or malicious access. Attacks on these assets are getting increasingly sophisticated and subtle, with the potential attack surface spanning clever exploitation of hardware, firmware, and hardware/software interfaces, and interception of device communication. The problem will get more critical and challenging in the future, with even more diversity in the device space including implants, wearables, and Internet-of-Things (IoTs), which, given their limited area and power budgets, do not permit many of the traditional hardware-based authentication and protection. To cope with these challenges, authentication mechanisms themselves are getting increasingly sophisticated, involving significant hardware/firmware interactions, which requires efficient design and test solutions and associated tools.

In this special session, we aim at providing comprehensive coverage of hardware authentication – spanning from ICs to IoTs. The first talk focuses on general hardware authentication primitives, their desired properties, and circuit-level implementation requirements. The second talk focuses on authentication requirements at system-on-chip (SoC) level focusing on associated policies and architecture. The third talk covers issues and emerging solutions related to IoT authentication.

4D.1 **PUF-Based Authentication**
Wenjie Che - Univ. of New Mexico
Fareena Saqib - Florida Institute of Technology
Jim Plusquellic - Univ. of New Mexico

4D.2 **Security Policy Enforcement in Modern SoC Designs**
Sandip Ray - Intel Corp.
Yier Jin - Univ. of Central Florida

4D.3 **Protecting Endpoint Devices in IoT Supply Chain**
Kun Yang, Domenic Forte, Mark M. Tehranipoor - Univ. of Florida

All speakers are denoted in bold | * denotes Best Paper Candidate
The Future of Energy-Efficient Computing

Dr. Stephen W. Keckler - NVIDIA Corporation

Time: 12:10pm - 1:20pm | Room: Phoenix Central

With the demise of Dennard scaling, the historical per-generation improvement in semiconductor fabrication technology has been cut in half. To obtain continued performance scaling, processor chips across the entire spectrum from embedded to datacenter computing must be more energy-efficient, more parallel, and at least as programmable as today’s serial processors. This talk will describe the principles behind NVIDIA’s GPU architectures, and present research concepts aimed at making such fine-grained parallel systems more efficient. It will also discuss the potential for innovations in signaling and packaging to provide new opportunities for efficient system architectures. Finally, it will describe the accelerating need for fast design time and the implications on design automation.

Biography:
Steve Keckler is a Senior Director of research at NVIDIA, where he leads the Architecture Research Group. He is also an Adjunct Professor of Computer Science at the University of Texas at Austin, where he served on the faculty from 1998-2012. His research interests include parallel computer architectures, high-performance computing, energy-efficient architectures, and embedded computing.

Dr. Keckler is a Fellow of the ACM, a Fellow of the IEEE, an Alfred P. Sloan Research Fellow, and a recipient of the NSF CAREER award, the ACM Grace Murray Hopper award, the President’s Associates Teaching Excellence Award at UT-Austin, and the Edith and Peter O’Donnell award for Engineering. He earned a B.S. in Electrical Engineering from Stanford University, and an M.S. and Ph.D. in Computer Science from the Massachusetts Institute of Technology.
5B - This Is How We Shrink
Time: 1:30pm - 3:30pm | Room: Dover's

Moderator:
Iris Hui-Ru Jiang - National Chiao Tung Univ.

This session provides early solutions to manufacturability issues arising at single-digit node technologies. Reducing the mask contribution to already challenging variability issues in a cost-effective manner is becoming critical. Shrinking pitch will necessitate the use of novel approaches, such as triple-patterning and introduction of directed-self assembly (DSA). We need to find ways to combine traditional yield improvement methods such as via redundancy with these new techniques.

The novel papers in this session are on TSP-based subfield scheduling methodology for e-beam photomask fabrication, triple-patterning-aware placement, DSA defect prediction and placement optimization, and redundant-via insertion for DSA.

5B.1 Provably Good Max-Min-m-neighbor-TSP-Based Subfield Scheduling for Electron-Beam Photomask Fabrication
Zhi-Wen Lin - National Taiwan Univ.
Shao-Yun Fang - National Taiwan Univ. of Science and Technology
Yao-Wen Chang, Wei-Cheng Rao, Chieh-Hsiung Kuan - National Taiwan Univ.

5B.2 Triple Patterning Aware Detailed Placement Toward Zero Cross-Row Middle-of-Line Conflict
Yibo Lin - Univ. of Texas at Austin
Bei Yu - Chinese Univ. of Hong Kong
Biying Xu, David Z. Pan - Univ. of Texas at Austin

5B.3 Defect Probability of Directed Self-Assembly Lithography: Fast Identification and Post-Placement Optimization
Seongbo Shim, Woohyun Chung, Youngsoo Shin - Korea Advanced Institute of Science and Technology

5B.4 Simultaneous Guiding Template Optimization and Redundant Via Insertion for Directed Self-Assembly
Shao-Yun Fang - National Taiwan Univ. of Science and Technology
Yun-Xiang Hong - National Taiwan Univ.
Yi-Zhen Lu - National Taiwan Univ. of Science and Technology

5C - State-Less Synthesis
Time: 1:30pm - 3:30pm | Room: Phoenix South

Moderator:
Zhiru Zhang - Cornell Univ.

This session presents new ideas in state-less synthesis that span approximate, physical and asynchronous synthesis. We start with a new, powerful way to realize and analyze approximate multipliers. The important problem of gate sizing is accelerated on a multi-core processor in the second paper. The last two contributions deal with asynchronous design. Starting with a signal transition protocol, the third paper synthesizes quasi-delay insensitive circuits. The last paper teaches how to convert a sequential circuit into an asynchronous design.

*5C.1 DRUM: A Dynamic Range Unbiased Multiplier for Approximate Applications
Soheil Hashemi, R. Iris Bahar, Sherief Reda - Brown Univ.

5C.2 Fast Lagrangian Relaxation Based Gate Sizing using Multi-Threading
Ankur Sharma - Iowa State Univ.
David Chinnery, Sarvesh Bhardwaj - Mentor Graphics Corp.
Chris Chu - Iowa State Univ.

5C.3 Asynchronous QDI Circuit Synthesis from Signal Transition Protocols
Bo-Yuan Huang, Yi-Hsiang Lai, Jie-Hong Roland Jiang - National Taiwan Univ.

5C.4 SPOCK: Static Performance Analysis and Deadlock Verification for Efficient Asynchronous Circuit Synthesis
Chun-Hong Shih, Yi-Hsiang Lai, Jie-Hong Roland Jiang - National Taiwan Univ.
Special Session 5D - The Landscape of Smart Buildings: Modeling, Management and Infrastructure

*Time: 1:30pm - 3:30pm | Room: Austin*

**Moderator:**
Yier Jin - Univ. of Central Florida

**Organizer:**
Xin Li - Carnegie Mellon Univ.

This special session is composed of four invited presentations to provide an in-depth treatment on both academic research and industrial development for smart buildings. The first talk describes learning based techniques to generate simple-yet-accurate thermal models for efficient building energy management. The second speaker introduces emerging CAD algorithms/methodologies for uncertainty analysis of smart buildings. The third presentation describes control and management methods to economically deliver energy to smart buildings/communities with consideration of security and privacy issues. Finally, the last speaker presents industrial perspectives on how to facilitate smart buildings within a smart grid.

5D.1 Learning Based Compact Thermal Modeling for Energy-Efficient Smart Building Management
Hengyang Zhao, Daniel Quach, Shujuan Wang - Univ. of California, Riverside
Haibao Chen - Shanghai Jiao Tong Univ.
Hai Wang - Univ. of Electronic Science and Technology of China
Xin Li - Carnegie Mellon Univ.
Sheldon X.-D. Tan - Univ. of California, Riverside

5D.2 From Robust Chip to Smart Building: CAD Algorithms and Methodologies for Uncertainty Analysis of Building Performance
Xiaoming Chen, Xin Li - Carnegie Mellon Univ.
Sheldon X.-D. Tan - Univ. of California, Riverside

5D.3 Security Analysis of Proactive Participation of Smart Buildings in Smart Grid
Tianshu Wei, Bowen Zheng, Qi Zhu - Univ. of California, Riverside
Shiyan Hu - Michigan Technological Univ.

5D.4 Buildings to Grid Integration: A Dynamic Contract Approach
Mehdi Maasoumy - C3 Energy
Alberto Sangiovanni-Vincentelli - Univ. of California, Berkeley

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6A - New CAD Directions for Emerging Technologies

*Time: 4:00pm - 6:00pm | Room: Phoenix North*

**Moderator:**
Hai (Helen) Li - Univ. of Pittsburgh

This session presents four interesting papers related to design automation for various emerging technologies. The first paper focuses on improving the reliability of 3D multi-level cell flash memory using a disturb-aware programming scheme. A power-efficient adaptive tuning technique is proposed in the second paper as a means to better manage bit-error rates in nanophotonic interconnects. Emerging technologies such as memristors, spintronic devices, and tunneling diodes can be used to build threshold logic gates. The third paper presents a pruning technique to more efficiently design circuits design from such gates. Finally, in the last paper, the temperature inversion effect is explored as a means of improving performance in finFET circuits.

6A.1 On Relaxing Page Program Disturbance over 3D MLC Flash Memory
Yu-Ming Chang, Yung-Chun Li - Macronix International Co., Ltd.
Yuan-Hao Chang - Academia Sinica
Tei-Wei Kuo - Academia Sinica & National Taiwan Univ.
Chih-Chang Hsieh, Hsiang-Pang Li - Macronix International Co., Ltd.

6A.2 Variation-Aware Adaptive Tuning for Nanophotonic Interconnects
Rui Wu - Univ. of California, Santa Barbara
Chin-Hui Chen, Cheng Li, Tsung-Ching Huang - Hewlett-Packard Labs
Fan Lan - Zhejiang Univ.
Chong Zhang - Univ. of California, Santa Barbara
Yun Pan - Zhejiang Univ.
John E. Bowers - Univ. of California, Santa Barbara
Ray Beausoleil - Hewlett-Packard Labs.
Kwang-Ting (Tim) Cheng - Univ. of California, Santa Barbara

6A.3 Threshold Logic Synthesis Based on Cut Pruning
Augusto Neutzling, Jody Maick Matos - Univ. Federal do Rio Grande do Sul
Alan Mishchenko - Univ. of California, Berkeley
Renato P. Ribas, Andre Reis - Univ. Federal do Rio Grande do Sul

6A.4 TEI-Turbo: Temperature Effect Inversion-Aware Turbo Boost for FinFET-Based Multi-Core Systems
Ermao Cai, Diana Marculescu - Carnegie Mellon Univ.
6B - Modern-Day Placement
Time: 4:00pm - 6:00pm | Room: Dover’s

Moderator:
Ismail Bustany - Mentor Graphics Corp.

Despite decades of academic and industrial research, placement still happens to be a highly relevant problem. Placement quality in large part decides the outcome of design closure. With an explosion in design size, complexity and design rules, placement needs to handle multiple objectives and constraints including routability, timing, power, and designer intent. The first two papers in this session address region constraints and detailed routability issues such as pin-access and pin-shorts during placement. The third paper tackles exploding design sizes by proposing an ultra-fast parallel global placement algorithm. The last paper optimizes timing in an incremental framework.

6B.1 Detailed-Routability-Driven Analytical Placement for Mixed-Size Designs with Technology and Region Constraints
Chau-Chin Huang, Hsin-Ying Lee, Bo-Qiao Lin, Sheng-Wei Yang, Chin-Hao Chang, Szu-To Chen, Yao-Wen Chang - National Taiwan Univ.

6B.2 High Performance Global Placement and Legalization Accounting for Fence Regions
Nima Karimpour Darav - Univ. of Calgary
Andrew Kennings - Univ. of Waterloo
David Westwick, Laleh Behjat - Univ. of Calgary

6B.3 POLAR 3.0: An Ultrafast Global Placement Engine
Tao Lin, Chris Chu, Gang Wu - Iowa State Univ.

6B.4 Exploiting Non-Critical Steiner Tree Branches for Post-Placement Timing Optimization
Vinicius Livramento, Chrystian Guth, Renan Netto, José Luis Güntzel, Luiz C. V. dos Santos - Federal Univ.of Santa Catarina

6C - Hardware Security: Methods and Metrics
Time: 4:00pm - 6:00pm | Room: Phoenix South

Moderators:
Saverio Fazzari - Booz Allen Hamilton, Inc.
Yier Jin - Univ. of Central Florida

This session discusses several aspects of hardware security. At the highest level of abstraction, paper 1 introduces a hardware framework for protecting the system from malicious third-party intellectual property, while paper 2 presents a methodology to detect firmware modifications for industrial control systems. Paper 3 introduces a new metric for assessing the susceptibility of a synthesized circuit to timing attacks. Paper 4 proposes the use of mutation testing for detecting hardware Trojans that exploit unspecified behavior in high-level specification of a design.

6C.1 A Flexible Architecture for Systematic Implementation of SoC Security Policies
Abhishek Basak, Swarup Bhunia - Case Western Reserve Univ.
Sandip Ray - Intel Corp.

6C.2 ConFirm: Detecting Firmware Modifications in Embedded Systems Using Hardware Performance Counters
Xueyang Wang, Charalambos Konstantinou - New York Univ.
Michail Maniatakos - New York Univ., Abu Dhabi
Ramesh Karri - New York Univ.

6C.3 Quantifying Timing-Based Information Flow in Cryptographic Hardware
Baolei Mao - Northwestern Polytechnical Univ.
Wei Hu, Alric Althoff, Janarbek Matal, Jason Oberg - Univ. of California at San Diego
Dejun Mu - Northwestern Polytechnical Univ.
Timothy Sherwood - Univ. of California, Santa Barbara
Ryan Kastner - Univ. of California at San Diego

6C.4 Detecting Hardware Trojans in Unspecified Functionality Using Mutation Testing
Nicole Fern, Kwang-Ting (Tim) Cheng - Univ. of California, Santa Barbara
6D - Variability, Noise, and Nonlinearity
Time: 4:00pm - 6:00pm | Room: Austin

Moderator:
Brian Mulvaney - Freescale Semiconductor, Inc.

This session showcases advances in dealing with variability, noise and nonlinearity challenges in analog and biological circuits. The first paper combines sparse regression with Bayesian model fusion to build efficient analog performance models. The second paper copes with the curse of dimensionality in Volterra modelling and simulation by employing low-rank tensor approximations. The third paper proposes techniques for efficient channel characterization of transceiver design. The last paper presents a number of innovations for simulating temporal noise in neuronal systems.

6D.1 A Sample Reduction Technique by Aliasing Channel Response for Fast Equalizing Transceiver Design
Sooeun Lee, Gunbok Lee, Jae-Yoon Sim, Hong-June Park, Wee Sang Park, Byungsub Kim - Pohang Univ. of Science and Technology

6D.2 Co-Learning Bayesian Model Fusion: Efficient Performance Modeling of Analog and Mixed-Signal Circuits Using Side Information
Fa Wang, Manzil Zaheer, Xin Li - Carnegie Mellon Univ.
Jean-Olivier Plouchart, Alberto Valdes-Garcia - IBM T.J. Watson Research Center

6D.3 STAVES: Speedy Tensor-Aided Volterra-Based Electronic Simulator
Haotian Liu, Xiaoyan Y. Z. Xiong, Kim Batselier, Lijun Jiang - Univ. of Hong Kong
Luca Daniel - Massachusetts Institute of Technology
Ngai Wong - Univ. of Hong Kong

6D.4 Simulation of Noise in Neurons and Neuronal Circuits
Deniz Kilinc, Alper Demir - Koc Univ.

Networking Reception
Time: 6:00pm - 6:30pm | Room: Prefunction Foyer

Whatever your goal, Networking Receptions are the perfect venue for you to expand your network and keep you connected! Join us today to catch up with your colleagues and discuss the day’s presentations with the conference presenters.

Reception is included with your conference registration fee.

ACM/SIGDA Member Meeting
Time: 6:30pm - 8:00pm | Room: Phoenix Central

The annual ACM/SIGDA Member Meeting will be held on Tuesday evening from 6:30-8pm. The meeting is open for ACM SIGDA members to attend. Members of the Electronic Design Automation community who would like to learn more about SIGDA or get involved with SIGDA activities are also invited. Dinner and beverages will be served.

The meeting will begin with a brief overview of our group, including its organization, activities, volunteering opportunities, member benefits. The 2015 ACM SIGDA Outstanding Young Faculty Award winner will present a talk to the audience and members at this event. Finally, we will end the evening with the announcement of this year’s winners of the ACM design automation Student Research Competition taking place at this year’s ICCAD. We hope to see you there!

Sponsored by:
<table>
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<tr>
<th>Time</th>
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| 8:00am - 9:15am | **Keynote: EDA Challenges and Opportunities with Emerging Applications and Technologies**  
|               | Dr. Renu Mehra, Synopsys, Inc. | Room: Phoenix Central |
| 9:30am - 10:00am | **Wednesday Fast Track Session**  
|               | Room: Phoenix Central |
| 10:00am - 10:30am | **Coffee Break**  
|               | Room: Prefunction Foyer |
| 10:30am - 12:00pm | **Session 7A: Embedded Software and Compilation Techniques for Power Efficiency**  
|               | Room: Phoenix North  
|               | **Session 7B: Design and Optimization of Cyberphysical Energy Systems**  
|               | Room: Dover's  
|               | **Session 7C: Synthesis and Methodology for Analog and Interconnect**  
|               | Room: Phoenix South  
|               | **Special Session 7D: Smart Chip for Smart Learning**  
|               | Room: Austin |
| 12:15pm - 1:15pm | **Lunch**  
|               | Room: Phoenix Central |
| 1:30pm - 3:30pm | **Session 8A: A New Perspective on MPSoC: From Memories to NoCs**  
|               | Room: Phoenix North  
|               | **Session 8B: Emerging Directions for Timing and Power Delivery Network Analysis**  
|               | Room: Dover's  
|               | **Session 8C: Remodel, Redesign, and Reconfigure for Reliability**  
|               | Room: Phoenix South  
|               | **Special Session 8D: Design for Big Data: From Architecture to Service - An Industrial Perspective**  
|               | Room: Austin |
| 3:30pm - 4:00pm | **Coffee Break**  
|               | Room: Prefunction Foyer |
| 4:00pm - 6:00pm | **Session 9A: Make or Break - Synthesis, Simulation and Post-Silicon Validation**  
|               | Room: Phoenix North  
|               | **Session 9B: Reducing Power and Lowering Temperature, Approximately!**  
|               | Room: Dover's  
|               | **Session 9C: Physical Optimization**  
|               | Room: Phoenix South  
|               | **Designer Track 9D: System Level Design Challenges and Solutions: From Memory to the Cloud**  
|               | Room: Austin |
| 5:30pm - 8:00pm | **Cocktail Reception + Synopsys AMS Special Interest Group Event: Addressing Advanced Simulation Challenges from Pure Analog to SoC and IoT Designs**  
|               | Location: Prefunction Foyer & Phoenix Central |
EDA Challenges and Opportunities with Emerging Applications and Technologies

Dr. Renu Mehra - Synopsys, Inc.

Time: 8:00am - 9:15am | Room: Phoenix Central

When the Mosaic browser was first released in 1993, few of us imagined the impact the internet would have on our daily lives. 20 years later, we stand at the cusp of another revolution, the cyber-physical one, and it is hard to fathom how our lives will change in the next 20 years.

With the internet of things, the digital/connected world meets physical objects that are everywhere, and digital electronics become ubiquitous, playing a much larger role in our lives. To be successful, these tiny ubiquitous devices must be able to harness power from the environment if possible and run with a very small power footprint. In the transportation sector, the automobile industry is moving aggressively to provide a more digital experience for drivers and passengers – from electric/hybrid powertrains, to infotainment, and advanced driver assist systems. In these systems, safety and reliability requirements for the electronic parts become paramount. In addition, the software component in these systems continues to increase; leaving us vulnerable to the hacks and security issues.

While the opportunities abound, the success of this new revolution will lie in whether we can solve the key challenges of low power, reliability, and security in an acceptable manner. The EDA industry is poised to play a key role in these areas. This talk will take a look at the possibilities and challenges that lie ahead.

Biography:
Dr. Renu Mehra is R&D Director for low-power implementation at Synopsys, Inc. Her interests include energy optimization with emphasis on addressing the needs of power-gates and multi-voltage designs. She leads a cross-functional team that addresses power optimization through different parts of the chip design flow including simulation, verification, and implementation. She has published several papers and books chapters on automated approaches for low power design and has authored three patents on this topic. She served as Program and General Chair of the IEEE/ACM International Symposium for Low Power Electronics and Design. She has participated in organizing positions, Technical Program Committees, tutorials, and panels in several EDA conferences and played a key role in the IEEE 1801 (UPF) standard. Before Synopsys, Dr. Mehra worked in a startup company, Clearwater Networks, on the design of an 8-way multi-threaded processor. Dr. Mehra received her Ph.D. and M.S. degrees in EECS from the University of California, Berkeley, and her Bachelor's degree in EE from the Indian Institute of Technology, Kanpur, India.
7B - Design and Optimization of Cyberphysical Energy Systems

**Time:** 10:30am - 12:00pm | **Room:** Dover’s

**Moderator:**
Wujie Wen - Florida International Univ.

This session introduces systematic design and optimization of cyberphysical energy systems, including solar energy harvesting systems, hybrid electrical vehicles and multi-tenant data centers. These papers apply a variety of design automation and optimization techniques such as stochastic modeling, machine learning and contract-based design to challenges in energy systems. The first paper introduces a stochastic model for energy management. The second paper minimizes the operating cost of hybrid electric vehicles through managing battery, ultracapacitor and battery cooling system. The third paper proposes a multi-tenant data center demand-side management using a contract design approach.

**7B.1 A Unified Stochastic Model for Energy Management in Solar-powered Embedded Systems**
Nga Dang, Roberto Valentini, Eli Bozorgzadeh, Marco Levorato, Nalini Venkatasubramanian - Univ. of California, Irvine

**7B.2 Machine Learning-Based Energy Management in a Hybrid Electric Vehicle to Minimize Total Operating Cost**
Xue Lin, Paul Bogdan - Univ. of Southern California
Naehyuck Chang - Korea Advanced Institute of Science and Technology
Massoud Pedram - Univ. of Southern California

**7B.3 A Contract Design Approach for Colocation Data Center Demand Response**
Kishwar Ahmed - Florida International Univ.
Mohammad Islam, Shaolei Ren - Univ. of California, Riverside

7C - Synthesis and Methodology for Analog and Interconnect

**Time:** 10:30am - 12:00pm | **Room:** Phoenix South

**Moderator:**
Eric Keiter - Sandia National Laboratories

The three papers in this session demonstrate innovative solutions towards new problems in analog circuit synthesis and emerging NEM relay and 3D circuits. The first paper develops automatic and fault-free synthesis of power-down circuits in analog/mixed-signal applications. A comprehensive set of models, tools and methodologies have been developed in the second paper for end-to-end evaluation of emerging NEM-relay based circuits. The last paper proposes a methodology for full-chip inter-die parasitic extraction in face-to-face-bonded 3D ICs.

**7C.1 Design Methodologies, Models and Tools for Very-Large-Scale Integration of NEM Relay-Based Circuits**
Tian Qin, Sunil Rana, Dinesh Pamunuwa - Univ. of Bristol

**7C.2 Full-chip Inter-die Parasitic Extraction in Face-to-Face-Bonded 3D ICs**
Yarui Peng, Taigon Song - Georgia Institute of Technology
Dusan Petranovic - Mentor Graphics Corp.
Sung Kyu Lim - Georgia Institute of Technology

**7C.3 Power-Down Circuit Synthesis for Analog/Mixed-Signal**
Michael Zwerger, Maximilian Neuner, Helmut Graeb - Technische Univ. München
Special Session 7D - Smart Chip for Smart Learning  
Time: 10:30am - 12:00pm | Room: Austin

**Moderator:**  
Xin Li - Carnegie Mellon Univ.

**Organizer:**  
Shawn Blanton - Carnegie Mellon Univ.

BIG DATA is everywhere and an emerging approach to deal with its vastness and complexity is through on-chip machine learning. The major objective of this special session is to: (1) introduce the technical background of on-chip machine learning to the VLSI-CAD community, (2) present the state-of-the-art technical challenges and open problems in this area, and finally (3) motivate VLSI-CAD researchers and professionals to pick up these emerging research problems and contribute to this promising and important area.

7D.1 Statistical Learning in Chip (SLIC)  
Shawn Blanton, Xin Li, Ken Mai, Diana Marculescu, Radu Marculescu, Jeyanandh Paramesh, Jeff Schneider, Donald E. Thomas - Carnegie Mellon Univ.

7D.2 Dynamic Machine Learning Based Matching of Nonvolatile Processor Microarchitecture to Harvested Energy Profile  
Kaisheng Ma, Xueqing Li - Pennsylvania State Univ.  
Yongpan Liu - Tsinghua Univ.  
John Sampson - Pennsylvania State Univ.  
Yuan Xie - Univ. of California, Santa Barbara  
Vijaykrishnan Narayanan - Pennsylvania State Univ.

7D.3 Architectural Requirements for Energy Efficient Execution of Graph Analytics Applications  
Mustafa Ozdal - Intel Corp. & Bilkent Univ.  
Serif Yesil - Bilkent Univ.  
Taemin Kim, Andrey Ayupov, Steven Burns - Intel Corp.  
Ozcan Ozturk - Bilkent Univ.

Lunch  
Time: 12:15 pm - 1:15pm | Room: Phoenix Central  
Join your friends and colleagues for lunch in Phoenix Central.

8A - A New Perspective on MPSoC: From Memories to NoCs  
Time: 1:30pm - 3:30pm | Room: Phoenix North

**Moderator:**  
Xin Li - Carnegie Mellon Univ.

This session presents a new perspective on how an MPSoC has to be designed. To meet performance and energy requirements it is necessary to rethink the way in which these architectures are envisioned. This new perspective has to embrace both memories and communication infrastructures.

First paper presents an Error-Correcting Code Generation for Non-Volatile Memories; second paper presents a critical application usage-aware memory system for mobile devices; third paper shows a universal ordered NoC design platform; finally, paper four is focused in optimizing 3D NoC design for energy efficiency.

8A.1 Bit-Write-Reducing and Error-Correcting Code Generation by Clustering Error-Correcting Codewords for Non-Volatile Memories  
Tatsuro Kojo, Masashi Tawada, Masao Yanagisawa, Nozomu Togawa - Waseda Univ.

8A.2 CAUSE: Critical Application Usage-Aware Memory System Using Non-volatile Memory for Mobile Devices  
Yeseong Kim, Mohsen Imani, Shruti Patil, Tajana Šimunić Rosing - Univ. of California at San Diego

8A.3 A universal ordered NoC design platform for shared-memory MPSoC  
Woo-Cheol Kwon, Li-Shiuuan Peh - Massachusetts Institute of Technology

8A.4 Optimizing 3D NoC Design for Energy Efficiency: A Machine Learning Approach  
Sourav Das, Janardhan Rao Doppa, Dae Hyun Kim, Partha Pande - Washington State Univ.  
Krishnendu Chakrabarty - Duke Univ.
8B - Emerging Directions for Timing and Power Delivery Network Analysis

Time: 1:30pm - 3:30pm | Room: Dover's

Moderators:
- Raju Balasubramanian - IBM Corp.
- Youngsoo Shin - Korea Advanced Institute of Science and Technology

Tasks of assessing a chip's timing performance and its power grid integrity are becoming increasingly challenging. The presentations in this session show some new directions to tackle these challenges.

The first paper estimates transient noise in power grid in a vector-less manner.

The second paper predicts resonance frequency of power delivery network using noise sensors. A Graph-based dynamic timing analysis method is emphasized in the third paper.

The last paper advances performance analysis for asynchronous designs.

8B.1 Transient Noise Bounds using Vectorless Power Grid Verification
Naval Gupte, Jia Wang - Illinois Institute of Technology

8B.2 1-Bit Compressed Sensing Based Framework for Built-in Resonance Frequency Prediction Using On-Chip Noise Sensors
Tao Wang, Jinglan Liu - Missouri Univ. of Science and Technology
Cheng Zhuo - Intel Corp.
Yiyu Shi - Univ. of Notre Dame

8B.3 Graph-based Dynamic Analysis: Efficient Characterization of Dynamic Timing and Activity Distributions
Hari Cherupalli, John Sartori - Univ. of Minnesota

8B.4 A General Framework for Efficient Performance Analysis of Acyclic Asynchronous Pipelines
Yi-Hsiang Lai, Chi-Chuan Chuang, Jie-Hong Roland Jiang - National Taiwan Univ.

8C - Remodel, Redesign, and Reconfigure for Reliability

Time: 1:30pm - 3:30pm | Room: Phoenix South

Moderator:
Saurabh Sinha - ARM, Inc.

The management of emerging reliability threats demands hierarchical innovations from technology modeling, circuit design, to architecture and computing algorithms. The first paper presents a TSV fatigue model that is based on the concept of entropy production. The second paper discusses opportunities and challenges in low power and reliable 3-tier 3D IC designs. The third paper offers ideas on how to use dual gates in FinFET cells to improve energy and reliability. The last paper presents efficient methods for the reconfiguration of FPGA interconnect to mitigate soft errors.

8C.1 A Novel Entropy Production Based Full-Chip TSV Fatigue Analysis
Tianchen Wang - Univ. of Notre Dame
Sandeep K. Samal, Sung Kyu Lim - Georgia Institute of Technology
Yiyu Shi - Univ. of Notre Dame

8C.2 Three-Tier 3D ICs for More Power Reduction: Strategies in CAD, Design, and Bonding Selection
Taigon Song - Georgia Institute of Technology
Shreepad Panth - Altera Corp.
Yoo-Jin Chae - Korea Advanced Institute of Science and Technology
Sung Kyu Lim - Georgia Institute of Technology

8C.3 Optimization of FinFET-based Circuits Using a Dual Gate Pitch Technique
Sravan K. Marella - Univ. of Minnesota, Twin Cities
Amit Ranjan Trivedi, Saibal Mukhopadhyay - Georgia Institute of Technology
Sachin S. Sapatnekar - Univ. of Minnesota

8C.4 Redundancy based Interconnect Duplication to Mitigate Soft Errors in SRAM-based FPGAs
Naifeng Jing, Jiacheng Zhou, Jianfei Jiang - Shanghai Jiao Tong Univ.
Xin Chen - Tongji Univ.
Weifeng He, Zhigang Mao - Shanghai Jiao Tong Univ.
Special Session 8D - Design for Big Data: From Architecture to Service - An Industrial Perspective

Time: 1:30pm - 3:30pm | Room: Austin

Moderator:
Zhuo Li - Cadence Design Systems, Inc.

Organizer:
Cheng Zhuo - Intel Corp.

With increasing system complexity and popularity of IoT/healthcare/WWW applications, data volume, velocity and variety are growing at an unprecedented pace. "Big data" is changing our daily life and has become one of the most concerning and important research areas for both hardware and software communities. Design for big data is an interactive procedure between software and hardware: New hardware and architecture designs must consider the challenges and specifications from the software stack to enable data sensing, collection, processing and distribution. On the other hand, software needs to fully utilize the hardware features/infrastructures for better performance and energy efficiency. Thus, this provides many open questions and opportunities for the CAD communities to bridge the interaction.

This special session consists of four invited talks and provides perspectives from leading hardware and software industries about potential research areas, interaction, and challenges for design for big data, spanning from architecture design, data processing and sorting to service concerns and specifications.

8D.1 Hardware Accelerator Design for Data Centers
Serif Yesil - Bilkent Univ.
Mustafa Ozdal - Intel Corp. & Bilkent Univ.
Taemin Kim, Andrey Ayupov, Steven Burns - Intel Corp.
Ozcan Ozturk - Bilkent Univ.

8D.2 Modern Big Data Analytics for "Old-fashioned" Semiconductor Industry Applications
Yada Zhu, Jinjun Xiong - IBM Research

8D.3 Effective CAD Research in the Sea of Papers
Jinglan Liu - Univ. of Notre Dame
Da-Cheng Juan - Google, Inc.
Yiyu Shi - Univ. of Notre Dame

8D.4 Dynamically Resilient and Agile Fine-Grained Replication Configuration
Yifang Liu - Google, Inc.

9A - Make or Break - Synthesis, Simulation and Post-Silicon Validation

Time: 4:00pm - 6:00pm | Room: Phoenix North

Moderator:
Miroslav Velev - Aries Design Automation, LLC

This session addresses correctness and verification at different levels of abstraction spanning synthesizing correct designs, transistor level simulation, and post-silicon validation.

The first paper uses the popular IC3/PDR to synthesize reactive systems. The second paper proposes a new data structure for symbolic timing simulation at transistor level. The third paper introduces an approach for non-repeating stimuli for post silicon constrained random verification. The final paper considers post-silicon coverage monitoring.

9A.1 Property-Directed Synthesis of Reactive Systems from Safety Specifications
Ting-Wei Chiang, Jie-Hong Roland Jiang - National Taiwan Univ.

9A.2 Efficient Transistor-Level Symbolic Timing Simulation Using Cached Partial Circuit States
Clayton McDonald, Hsinwei Chou, Vijay Durairaj, Pey-Chang Kent Lin - Synopsys, Inc.

9A.3 On-Chip Generation of Uniformly Distributed Constrained-Random Stimuli for Post-Silicon Validation
Xiaobing Shi, Nicola Nicolici - McMaster Univ.

9A.4 Reducing Post-Silicon Coverage Monitoring Overhead with Emulation and Bayesian Feature Selection
Ricardo Ochoa Gallardo, Alan J. Hu, André Ivanov - Univ. of British Columbia
Maryam S. Mirian - Univ. of Tehran
9B - Reducing Power and Lowering Temperature, Approximately!

Time: 4:00pm - 6:00pm | Room: Dover’s

Moderator:
Muhammad Shafique - Karlsruhe Institute of Technology

This session focuses on the state-of-the-art in thermal management and low power design techniques. The first paper proposes a technique to trade-off quality for energy using approximate computing. The next two papers propose new thermal modeling and mitigation techniques for mobile devices. A paper on machine-learning based power modeling of black-box IPs wraps up the session.

9B.1 ApproxEigen: An Approximate Computing Technique for Large-Scale Eigen-Decomposition
Qian Zhang, Ye Tian, Ting Wang, Feng Yuan, Qiang Xu - Chinese Univ. of Hong Kong

9B.2 Modeling and Mitigation of Extra-SoC Thermal Coupling Effects and Heat Transfer Variations in Mobile Devices
Francesco Paterna, Tajana Šimunić Rosing - Univ. of California at San Diego

9B.3 Just Enough is More: Achieving Sustainable Performance in Mobile Devices Under Thermal Limitations
Onur Sahin, Paul Thomas Varghese, Ayse K. Coskun - Boston Univ.

9B.4 Learning-Based Power Modeling of System-Level Black-Box IPs
Dongwook Lee - Univ. of Texas at Austin
Taemin Kim, Kyungtae Han, Yatin Hoskote - Intel Corp.
Lizy John, Andreas Gerstlauer - Univ. of Texas at Austin

9C - Physical Optimization

Time: 4:00pm - 6:00pm | Room: Phoenix South

Moderator:
Chuck Alpert - Cadence Design Systems, Inc.

The papers in this session present physical design techniques that optimize timing, power, and area for advanced technologies. The first paper presents a design flow to integrate standard cells of mixed heights at a fine-grained level to optimize area and power. The second paper targets leakage power saving in multiple power design domains by clustering buffers of inter-region nets together on the layout. The third paper presents a mathematical formulation for detailed placement to model advanced technology nodes. The last paper presents a generic routing framework in microfluidic biochips to optimize number of time steps or pin count.

9C.1 Mixed Cell-Height Implementation for Improved Design Quality in Advanced Nodes
Sorin Dobre - Qualcomm Technologies, Inc.
Andrew B. Kahng, Jiajia Li - Univ. of California at San Diego

9C.2 GasStation: Power and Area Efficient Buffering for Multiple Power Domain Design
Chien-Pang Lu - MediaTek, Inc.
Iris Hui-Ru Jiang - National Chiao Tung Univ.
Chin-Hsiung Hsu - MediaTek, Inc.

9C.3 Scalable Detailed Placement Legalization for Complex Sub-14nm Constraints
Kwangsoo Han, Andrew B. Kahng, Hyein Lee - Univ. of California at San Diego

9C.4 A General and Exact Routing Methodology for Digital Microfluidic Biochips
Oliver Keszocze, Robert Wille - Univ. of Bremen & DFKI GmbH
Krishnendu Chakrabarty - Duke Univ.
Rolf Drechsler - Univ. of Bremen & DFKI GmbH
Designer Track 9D - System Level Design Challenges and Solutions: From Memory to the Cloud

*Time: 4:00pm - 6:00pm | Room: Austin*

**Moderators:**
- Yuan Xie - Univ. of California, Santa Barbara
- Sri Parameswaran - Univ. of New South Wales

This Designer Track session will examine system level concerns of modern and future designs as seen from the perspective of four speakers with vast industry experience (from Huawei, HP Labs, AMD, and IBM). The first speaker will delve into approaches to Cognitive Cloud Platforms with particular emphasis on computation, storage, and communication. The second speaker will discuss various aspects of forthcoming designs, including technology trends, managing data, and software implications. The third speaker will look at some of the transformational memory technologies and discuss the niches where these might be applied. Finally, the last speaker will examine the resilience challenges posed by data centers and the techniques used to overcome them.

9D.1  C^4 - Cases for Cognitive Computing Cloud

Jian Li - Huawei Technologies Co., Ltd.

9D.2  Memory Driven Computing: A New Architecture for the Data-centric World

Paolo Faraboschi - Hewlett-Packard Labs.

9D.3  Interface and Developmental Challenges for Emerging Memory Technologies

Michael Ignatowski - Advanced Micro Devices, Inc.

9D.4  Resilience at Scale - Insights and Opportunities

Sudhanva Gurumurthi - Cloud Innovation Lab, IBM Corp.

Cocktail Reception + Synopsys AMS Special Interest Group Event: Addressing Advanced Simulation Challenges from Pure Analog to SoC and IoT Designs

*Time: 5:30pm - 8:00pm | Room: Prefunction Foyer & Phoenix Central*

In today’s environment, analog/mixed-signal IC designers face challenges at multiple levels that range from device modeling and reliability analysis to complex mixed-signal verification. To address these challenges, Synopsys continues to enhance its broad portfolio of circuit simulation solutions to accommodate the higher performance, capacity and complexity required by advanced designs and process technologies.

Join us for the AMS Special Interest Group (SIG) event during ICCAD where our panel of industry-leading experts from semiconductor companies will present their circuit simulation flows and methodologies that address advanced design challenges and enable them to bring products to market more quickly and efficiently.

5:30pm – 6:30pm - Cocktail Reception
6:30pm – 7:45pm - Dinner and Technical Presentations
7:45pm – 8:00pm - Conclusion and Prize Drawings

Attendance at this event is free, but registration is required.

Sponsored by:

All speakers are denoted in bold | * denotes Best Paper Candidate
- THURSDAY & FRIDAY WORKSHOPS -

8:00am - 5:00pm
Workshop 1: Hardware and Algorithms for Learning On-a-Chip (HALO)
   Room: Phoenix North | Thursday Only

8:00am - 6:00pm
Workshop 4: Frontiers in Analog CAD
   Room: Austin | Thursday & Friday

8:45am - 5:30pm
Workshop 5: 8th IEEE/ACM Workshop on Variability Modeling and Characterization
   Room: Phoenix South | Thursday Only

9:00am - 5:15pm
Workshop 2: Ninth International Workshop on Constraints in Formal Verification (CFV’15)
   Room: Dover’s | Thursday Only

Workshop 1 - Hardware and Algorithms for Learning On-a-Chip (HALO)
Time: 8:00am - 5:00pm | Room: Phoenix North

Organizers:
   Yu Cao - Arizona State Univ.
   Xin Li - Carnegie Mellon Univ.
   Jieping Ye - Univ. of Michigan

Machine learning algorithms, such as those for image based search, face recognition, multi-category classification, and scene analysis, are being developed that will fundamentally alter the way individuals and organizations live, work, and interact with each other. However their computational complexity still challenges the state-of-the-art computing platforms, especially when the application of interest is tightly constrained by the requirements of low power, high throughput, small latency, etc.

In recent years, there have been enormous advances in implementing machine learning algorithms with application-specific hardware (e.g., FPGA, ASIC, etc.). There is a timely need to map the latest learning algorithms to physical hardware, in order to achieve orders of magnitude improvement in performance, energy efficiency and compactness.

Recent progress in computational neurosciences and nanoelectronic technology, such as resistive memory devices, will further help shed light on future hardware-software platforms for learning on-a-chip.

The overarching goal of this workshop is to explore the potential of on-chip machine learning, to reveal emerging algorithms and design needs, and to promote novel applications for learning. It aims to establish a forum to discuss the current practices, as well as future research needs.

Speakers:
   Jason Cong - Univ. of California, Los Angeles
   Eugenio Culurciello - Purdue Univ.
   Eric Chung - Microsoft Research
   Jian Li - Huawei Technologies Co., Ltd.
   Yasuki Tanabe - Toshiba Corp.
   Martin Woolf - Raytheon Company
   Peter Chin - Charles Stark Draper Laboratory
   Jeff Schneider - Uber Technologies, Inc.
   Andrew Cassidy - IBM Research - Almaden
   Gert Cauwenberghs - Univ. of California at San Diego
   Damien Querlioz - Centre National de la Recherche Scientifique

Sponsored by:
Workshop 2 - Ninth International Workshop on Constraints in Formal Verification (CFV'15)

**Time:** 9:00am - 5:15pm | **Room:** Dover's

**General Chair:**
Miroslav Velev - Aries Design Automation, LLC

**Workshop Chair:**
Alex Groce - Oregon State Univ.

**Publicity Chair:**
Kristin Yvonne Rozier - Univ. of Cincinnati

Formal verification is of crucial significance in the development of hardware and software systems. In the last decade, tremendous progress was made in both the speed and capacity of constraint technology. Most notably, Boolean Satisfiability (SAT) solvers have become orders of magnitude faster and capable of handling problems that are orders of magnitude bigger, thus enabling the formal verification of more complex computer systems. As a result, the formal verification of hardware and software has become a promising area for research and industrial applications. Constraints have applications to all formal verification methods. Particularly, the efficient use of constraints can make or break a formal verification run, and can result in orders of magnitude speedup and orders of magnitude increase in scalability for solving of larger problems.

The main goal of the Constraints in Formal Verification workshop is to bring together researchers from the CSP/SAT and the formal verification communities, to describe new applications of constraint technology to formal verification, to disseminate new challenging problem instances, and to propose new dedicated algorithms for hard formal verification problems. This workshop will be of interest to researchers from both academia and industry, working on constraints or on formal verification and interested in the application of constraints to formal verification.

Workshop 3 - Workshop on Efficient Computing in the Dark Silicon Era

**Time:** 8:00am - 6:00pm | **Room:** Phoenix Central

**Organizers:**
Muhammad Shafique - Karlsruhe Institute of Technology
Mustafa Ozdal - Bilkent Univ.
Gi-Joon Nam - IBM Corp.
Siddharth Garg - New York Univ.

Current semiconductor scaling trends indicate that in future technology nodes, a significant fraction of the chip would have to be kept powered off to meet peak power and thermal constraints. This is referred to as the dark silicon problem.

The dark silicon problem introduces new challenges for EDA, low-power design and micro-architecture research across design abstractions (ranging from devices and circuits to micro-architecture and the system level). In particular, how to best utilize the abundance of (potentially dark) transistors, both in terms of design time provisioning and run-time management, so as to improve quality metrics (performance, reliability, lifetime, etc.) within peak power and thermal constraints. Indeed, dark Silicon processors are envisaged to be designed different from the largely homogeneous multi-cores commercially available today and will instead feature a heterogeneous mix of computing and communication resources to achieve higher performance and better power/energy/thermal efficiency.

This workshop is intended to be a forum to synthesize emerging perspectives and research directions on the dark silicon problem from across industry and academia.
Workshop 4 - Frontiers in Analog CAD  
*Time: 8:00am - 5:00pm | Room: Austin*  

**Organizers:**  
Xin Li - Carnegie Mellon Univ.  
Scott Little - Intel Corp.  
Helmut Graeb - Technische Univ. München  

This workshop occurs on both Thursday and Friday:  
Thursday, November 5: 8:00am - 5:00pm  
Friday, November 6: 8:00am - 12:00pm  

Growing digitization of integrated circuits has contributed to making system-on-chips ever more complex. Yet, it does not prevent that a substantial portion of a chip consists of analog and mixed-signal (AMS) circuits that provide critical functionality like signal conversion. Aggressive scaling of IC technologies, as well as advancing the integration of heterogeneous physical domains on chip, substantially complicates the design of AMS components.

On the one hand, their modeling and design becomes extremely complex. On the other hand, their interplay with the rest of the system-on-chip challenges design, verification and test. The new technology trends bring up enormous challenges and opportunities for AMS design automation. This is reflected by an increase in research activity on AMS CAD worldwide. The purpose of this workshop is to bring together academic and industrial researchers from both design and CAD communities to report recent advances and motivate new research topics and directions in this area.

**Workshop 5: 8th IEEE/ACM Workshop on Variability Modeling and Characterization**  
*Time: 8:45am - 5:30pm | Room: Phoenix South*  

**Organizers:**  
Rasit Topaloglu - IBM Corp.  
Takashi Sato - Kyoto Univ.  
Jaijeet Roychowdhury - Univ. of California, Berkeley  

Variability has emerged as a fundamental challenge to IC design in scaled CMOS technology; and it has profound impact on nearly all aspects of circuit performance. While some of the negative effects of variability can be handled via improvements in the manufacturing process, comprehensive methods are necessary to assess and manage the negative effects of variability, which in turn requires accurate and tractable variability models. The goal of the VMC workshop is to provide a forum for theoreticians and practitioners to freely exchange opinions on current practices as well as future research needs in variability modeling and characterization. This year VMC is co-organized with NSF-SRC NEEDS.

**Topics**  
1. Fundamental physics of device variability  
2. Compact variability modeling development and applications  
3. Statistical extraction of variability  
4. Variability test structure design and calibration  
5. Design interface with manufacturing and solutions for variability  
6. Variability issues in emerging semiconductor technology  
7. Temporal variability issues  
8. Reliability considerations that may be closely related to variability  
9. Variability in computing and systems  

**Speakers:**  
Mark Lundstrom - Purdue Univ.  
Xin Li - Carnegie Mellon Univ.  
Muhammad Ashraf Alam - Purdue Univ.  
Hiroyuki Matsui - Univ. of Tokyo  
Swarup Bhunia - Univ. of Florida  
Runsheng Wang - Peking Univ.  
Zheng Zhang - Massachusetts Institute of Technology  

**Sponsored by:**

IEEE, CEDA, cadence, Intel, ACM, Association for Computing Machinery, NEEDS
Workshop 4 - Frontiers in Analog CAD
Time: 8:00am - 12:00pm | Room: Austin

Organizers:
Xin Li - Carnegie Mellon Univ.
Scott Little - Intel Corp.
Helmut Graeb - Technische Univ. München

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For more information on CEDA, visit: ieee-ceda.org.

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