# Monday Schedule

**8:00am - 8:30am**
Opening Session & Awards  
*Room: Phoenix Central*

**8:30am - 9:15am**
**Keynote:** Computing for Robots and Biomolecules  
*Lydia E. Kavraki, Rice Univ.*  
*Room: Phoenix Central*

**9:30am - 10:00am**
Monday Fast Track Session  
*Room: Phoenix Central*

**10:00am - 10:30am**
Coffee Break  
*Room: Prefunction Foyer*

**10:30am - 12:00pm**
Session 1A: Machine Learning in VLSI Design, Yield Estimation and Post-Silicon Validation  
*Room: Phoenix North*

Session 1B: Optimization Techniques for Upcoming Embedded Systems  
*Room: Dover’s*

Special Session 1C: Self-aware Systems-on-Chip  
*Room: Phoenix South*

Embedded Tutorial 1D: Formal Methods for Emerging Technologies  
*Room: Austin*

**11:30am - 1:30pm**
ACM Student Research Competition Poster Session  
*Room: DeZavala*

**1:30pm - 3:30pm**
Session 2A: High-Level and Sequential Synthesis  
*Room: Phoenix North*

Session 2B: Keep Austin Wired: Routing and Clocking  
*Room: Dover’s*

Session 2C: Hardware Based Authentication  
*Room: Phoenix South*

Special Session 2D: Dennard Scaling is History and Moore’s Law is Aging: How to Break the Inevitable Power Wall?  
*Room: Austin*

**3:00pm - 4:00pm**
Coffee Break  
*Room: Prefunction Foyer*

**4:00pm - 5:30pm**
Session 3A: Design Automation for Non-Traditional Architectures  
*Room: Phoenix North*

Session 3B: Modeling, Optimization, and Synthesis of Cyberphysical Systems  
*Room: Dover’s*

Session 3C: The Art of Engineering Heterogeneous Computing Systems  
*Room: Phoenix South*

Special Session 3D: From EDA to DA: Can We Evolve Beyond Our E-Roots?  
*Room: Austin*

**5:30pm - 6:00pm**
Networking Reception  
*Room: Prefunction Foyer*

**6:00pm - 6:55pm**
Special Session 10A: TAU 2015 Contest on Incremental Timing and CPPR Analysis  
*Room: Phoenix North*

**6:00pm - 7:30pm**
Special Session 10D: Rebooting Computing and Low Power Image Recognition Challenge  
*Room: Austin*

**7:05pm - 8:30pm**
Special Session 10B: 2015 CAD Contest  
*Room: Phoenix North*
- OPENING SESSION & AWARD PRESENTATIONS -

Time: 8:00am - 8:30am | Room: Phoenix Central

Kick off the conference with opening remarks from the ICCAD Executive Committee members and hear the highlights of the conference. The IEEE/ACM William J. McCalla ICCAD Best Paper award will be announced along with other award presentations from IEEE and ACM.

IEEE/ACM William J. McCalla ICCAD Best Paper Award
This award is given in memory of William J. McCalla for his contributions to ICCAD and his CAD technical work throughout his career.

Front-End Award:
  Session 5A.1: A Polyhedral-based SystemC Modeling and Generation Framework for Effective Low-power Design Space Exploration  
  Wei Zuo, Warren Kemmerer, Jong Bin Lim - Univ. of Illinois at Urbana-Champaign  
  Louis-Noël Pouchet - Ohio State Univ.  
  Andrey Ayupov, Taemin Kim, Kyungtae Han - Intel Corp.  
  Deming Chen - Univ. of Illinois at Urbana-Champaign

Back-End Award:
  Session 4B.2: Defect Clustering-Aware Spare-TSV Allocation for 3D ICs  
  Shengcheng Wang, Mehdi Tahoori - Karlsruhe Institute of Technology  
  Krishnendu Chakrabarty - Duke Univ.

Ten Year Retrospective Most Influential Paper Award
This award is being given to the paper judged to be the most influential on research and industrial practice in computer-aided design over the ten years since its original appearance at ICCAD.

2005 Paper Titled: Performance Analysis of Carbon Nanotube Interconnects for VLSI Applications  
  Navin Srivastava, Kaustav Banerjee - Univ. of California, Santa Barbara

IEEE Fellow
Diana Marculescu - Carnegie Mellon Univ.  
For contributions to design and optimization of energy-aware computing systems.

IEEE CEDA Outstanding Service Award
Yao-Wen Chang - National Taiwan Univ.  
For outstanding service to the EDA community as ICCAD General Chair in 2014.

IEEE CEDA Ernest S. Kuh Early Career Award
Zhiru Zhang - Cornell Univ.  
For outstanding contributions to algorithms, methodologies, and successful commercialization of high-level synthesis tools for FPGAs.

ACM/SIGDA CADathlon
Introduction of the 2015 winners.
- KEYNOTE ADDRESS -

Computing for Robots and Biomolecules

Lydia E. Kavraki - Rice Univ.

Time: 8:30am - 9:15am | Room: Phoenix Central

Over the last decade, the development of fast and reliable motion planning algorithms has deeply influenced many domains in robotics, such as industrial automation and autonomous exploration. Motion planning has also contributed to great advances in an array of unlikely fields, including graphics animation and computational structural biology.

This talk will first describe how sampling-based methods revolutionized motion planning in robotics. The presentation will quickly focus on recent algorithms that are particularly suitable for systems with complex dynamics. The talk will then introduce an integrative framework that allows the synthesis of motion plans from high-level specifications. The framework uses temporal logic and formal methods and establishes a tight link between classical motion planning in robotics and task planning in artificial intelligence. Although research initially began in the realm of robotics, the experience gained has led to algorithmic advances for analyzing the motion and function of proteins, the worker molecules of all cells. This talk will conclude by discussing robotics-inspired methods for computing the flexibility of proteins and large macromolecular complexes with the ultimate goals of deciphering molecular function and aiding the discovery of new therapeutics.

Biography:
Lydia E. Kavraki is the Noah Harding Professor of Computer Science and Professor of Bioengineering at Rice University. She received her B.A. in Computer Science from the University of Crete in Greece and her Ph.D. from Stanford University. Her research focuses on physical algorithms and their applications in robotics, computational structural biology, and translational bioinformatics.

Kavraki has authored more than 200 peer-reviewed journal and conference publications and is one of the authors of the widely-used robotics textbook titled "Principles of Robot Motion" published by MIT Press. Kavraki currently serves as an associate editor for several journals including the International Journal of Robotics Research, the ACM/IEEE Transactions on Computational Biology and Bioinformatics, Frontiers in Molecular Biosciences, and Springer Tracts in Advanced Robotics. She is the recipient of the 2000 Association for Computing Machinery (ACM) Grace Murray Hopper Award, a Fellow of ACM, IEEE, AAAS, AAAI, AIMBE, and a member of the National Academy of Medicine.

Monday Fast Track Session

Time: 9:30am - 10:00am | Room: Phoenix Central

Get on the Fast Track to Monday with a 45-second preview of upcoming presentations for the day.

1A - Machine Learning in VLSI Design, Yield Estimation and Post-Silicon Validation

Time: 10:30am - 12:00pm | Room: Phoenix North

Moderator:
Abe Elfadel - Masdar Institute of Science and Technology

This session is devoted to machine learning algorithms in VLSI design, yield prediction, and post-silicon validation.

The first paper in this session applies Google's PageRank algorithm to RTL designs to significantly improve the behavioral coverage of signals for post-silicon debug. The second paper applies Bayesian learning to the problem of yield prediction when a VLSI design is migrated from a source fab to a target fab. Finally, the third paper proposes a novel architecture for algorithmic noise tolerance that results in significant improvement in the resiliency and energy efficiency of machine-learning kernel implementations.

1A.1 Can't See the Forest for the Trees: State Restoration's Limitations in Post-silicon Trace Signal Selection

Sai Ma, Debjit Pal, Rui Jiang - Univ. of Illinois at Urbana-Champaign

Shobha Vasudevan - Univ. of Illinois at Urbana-Champaign

1A.2 Yield Forecasting in Fab-to-Fab Production Migration Based on Bayesian Model Fusion

Ali Ahmad - Univ. of Texas at Dallas

Haralampos-G. Stratigopoulos - LIP6 Laboratory, CNRS, Univ. Pierre et Marie Curie

Amit Nahar, Bob Orr, Michael Pas - Texas Instruments, Inc.

Yiorgos Makris - Univ. of Texas at Dallas

1A.3 Reduced Overhead Error Compensation for Energy Efficient Machine Learning Kernels

Sai Zhang, Naresh Shanbhag - Univ. of Illinois at Urbana-Champaign

All speakers are denoted in bold | * denotes Best Paper Candidate
**1B - Optimization Techniques for Upcoming Embedded Systems**

*Time: 10:30am - 12:00pm | Room: Dover’s*

**Moderator:**
Andreas Gerstlauer - Univ. of Texas at Austin

This session addresses new challenges posed by emerging memory technologies, and runtime reconfigurable solutions.

The first paper in the session focuses on a light-weight controller for PCM-based main memory technologies that exploit TLB miss information. The second paper proposes reshaping of access patterns for embedded multi-media controllers for solid-state drives. The third paper proposes a stress-aware placement technique to mitigate aging for reconfigurable architectures.

1B.1 A Light-Weighted Software-Controlled Cache for PCM-based Main Memory Systems
Hung-Sheng Chang - National Taiwan Univ.
Yuan-Hao Chang - Academia Sinica
Tei-Wei Kuo - Academia Sinica & National Taiwan Univ.
Hsiang-Pang Li - Macronix International Co., Ltd.

1B.2 Access Pattern Reshaping for eMMC-enabled SSDs
Chien-Chung Ho - National Taiwan Univ.
Yuan-Hao Chang - Academia Sinica
Tei-Wei Kuo - Academia Sinica & National Taiwan Univ.

1B.3 STRAP: Stress-Aware Placement for Aging Mitigation in Runtime Reconfigurable Architectures
Hongyan Zhang - Karlsruhe Institute of Technology
Michael A. Kochte, Eric Schneider - Univ. of Stuttgart
Lars Bauer - Karlsruhe Institute of Technology
Hans-Joachim Wunderlich - Univ. of Stuttgart
Jörg Henkel - Karlsruhe Institute of Technology

**Special Session 1C - Self-aware Systems-on-Chip**

*Time: 10:30am - 12:00pm | Room: Phoenix South*

**Moderator:**
Ulf Schlichtmann - Technische Univ. München

**Organizer:**
Mehdi B. Tahoori - Karlsruhe Institute of Technology

While the notion of self-awareness has a long history in biology, psychology, medicine, engineering and (more recently) computing, we are seeing the emerging need for self-awareness in the context of complex many-core Systems-on-Chip that must address the often conflicting requirements of performance, resiliency, energy, heat, cost, security, etc. in the face of highly dynamic operational behaviors coupled with process, environment, and workload variabilities. Unlike traditional MultiProcessor Systems-on-Chip (MPSoCs), self-aware SoCs must deploy an intelligent co-design of the control, communication, and computing infrastructure that interacts with the physical environment in real-time in order to modify the system’s behavior so as to adaptively achieve desired objectives and Quality-of-Service (QoS). Self-aware SoCs require a combination of ubiquitous sensing and actuation, health-monitoring, and statistical model-building to enable the SoC’s adaptation over time and space. Accordingly, this special session first outlines the notions of self-awareness in computing and then features three different dimensions of self-aware Systems-on-Chip.

The first talk by Prof. Nikil Dutt defines the notion of self-aware computing and presents the Cyber-Physical System-on-Chip (CPSoC) concept as an exemplar of a self-aware SoC that intrinsically couples on-chip and cross-layer sensing and actuation using a sensor-actuator rich fabric to enable self-awareness. The second talk by Prof. Mehdi Tahoori discusses data-driven learning based chip health monitoring infrastructure to ensure system resilience. The third talk by Prof. Abhijit Chatterjee presents self-aware self-learning real-time systems with applications to wireless communication, signal processing and control.

1C.1 Self-Aware Cyber-Physical Systems-on-Chip
Nikil Dutt - Univ. of California, Irvine
Axel Jantsch - Technische Univ. Wien
Sanatnud Sarma - Univ. of California, Irvine

1C.2 Fine-Grained Aging Prediction Based on the Monitoring of Run-Time Stress Using DfT Infrastructure
Abhishek Koneru - Duke Univ.
Arunkumar Vijayan - Karlsruhe Institute of Technology
Krishnendu Chakrabarty - Duke Univ.

1C.3 Self Learning Analog/Mixed-Signal/RF Systems: Dynamic Adaptation to Workload and Environmental Uncertainties
Debashis Banerjee, Shreyas Sen, Abhijit Chatterjee - Georgia Institute of Technology
Embedded Tutorial 1D - Formal Methods for Emerging Technologies

*Time: 10:30am - 12:00pm | Room: Austin*

**Moderator:**
Rolf Drechsler - Univ. of Bremen & DFKI GmbH

**Organizer:**
Robert Wille - Univ. of Bremen & DFKI GmbH

Formal Methods advanced to an important core technology in Computer-Aided Design (CAD). At the same time, researchers and engineers also started the investigation of so-called emerging technologies such as quantum computation, reversible computation, optical circuits, or biochips. Although most of these technologies are still in a rather “academic” state, first physical realizations have already been presented or even entered the market recently. This motivates a more detailed consideration of how to design circuits for these technologies. As for conventional circuits, formal methods do play an important role here.

In this tutorial, we are aiming to address the current momentum caused by the recent accomplishments and provide a comprehensive introduction into these emerging technologies as well as their corresponding CAD methods. This will include a special focus on how formal methods may help in the design and verification of circuits for those technologies.

**1D.1 Formal Methods for Emerging Technologies**

Robert Wille - Univ. of Bremen & DFKI GmbH

Rolf Drechsler - Univ. of Bremen & DFKI GmbH

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ACM Student Research Competition Poster Session

*Time: 11:30am - 1:30pm | Room: DeZavala*

**Organizers:**
Tsung-Yi Ho - National Tsing Hua Univ.
Yiyu Shi - Univ. of Notre Dame

Sponsored by Microsoft Research, the ACM Student Research Competition (SRC) is an internationally recognized venue enabling undergraduate and graduate students who are members of ACM and ACM SIGDA to:

- Experience the research world—for many undergraduates this is a first!
- Share research results and exchange ideas with other students, judges, and conference attendees.
- Rub shoulders with academic and industry luminaries.
- Understand the practical applications of their research.
- Perfect their communication skills.
- Receive prizes and gain recognition from ACM, and the greater computing community.

ACM SRC has three rounds:
1. Abstract review
2. Poster session (this session)
3. Technical presentation

In the first round, 2-page research abstracts are evaluated by EDA experts from academia and industry to select participants for the second round (this session). For the ACM SRC at ICCAD 2015 competition, 20 participants were invited to present their research at ICCAD.

The posters are evaluated by EDA experts to select 5 participants in graduate and undergraduate categories to advance to the final round (technical presentation round). Students are expected to discuss their work with judges. Each judge will rate the student’s visual presentation based on the criteria of uniqueness of the approach, the significance of the contribution, visual presentation, and quality of presentation.

More details can be found at sigda.org/src.
From Boolean Algebra to Basketball: Applying EDA Techniques to Sports Analytics

Charles J. Alpert - Cadence Design Systems, Inc.

Time: 12:15pm - 1:15pm | Room: Phoenix Central

Professional sports are big business. The National Football League generates over ten billion dollars annually, but this is actually less than fantasy sports, which generates 15 billion in revenue (about double the entire EDA industry). Not surprisingly, the interest in utilizing data analytics for sports applications has exploded in recent years. The algorithm techniques utilized share significant overlap with traditional EDA algorithms. Win and playoff prediction tools utilize Monte Carlo simulation. Similar to how model-order reduction can produce simplified circuits, analytic techniques aggregate mountains of player statistics to model the a player’s actual value. In this talk, we describe how EDA techniques can be applied to college basketball, or more specifically, the NCAA tournament.

Each March, the NCAA tournament pits 64 of the best college basketball teams into a single elimination tournament to determine the national champion. The first round has 32 matches, the second round has 16 matches, and so on, until a single champion emerges. Millions of fans, including President Obama, participate in “bracketology” pools in which they predict the winners for each of these 63 matches. Millions of participants enter their picks on sports media websites hoping to earn office bragging rights or to win major prizes. Once the tournament starts, automatic software tracks contestants’ correct picks, their maximum score, and their current place in the standings. However, today’s websites lack sufficient information to show participants how they are performing. This talk shows how simulation can be used to determine each participants probability of winning. We also discuss how logic synthesis can be applied to determine the exact winning scenarios for each participant. Finally, the talk will present other sports problems which are suitable for algorithmic innovation.

Biography:
Charles (Chuck) Alpert joined Cadence Design Systems in 2014, where he serves as a Group Director for the Digital Signoff Group. His team researches and develops next generation algorithms, solutions, and methodologies for Cadence's digital implementation tools. Prior to that, Chuck spent 17 years working for the IBM Research Division, developing internal EDA tools in the physical design space. He received a Ph.D. in Computer Science from UCLA in 1996 and a B.S. and a B.A. degree from Stanford in 1991. Chuck’s interests include algorithms for placement, routing, wire synthesis, clocking and for sports analysis. He is an IEEE Fellow and has published over 100 conference and journal publications and has filed 100 patents. He currently serves as Deputy Editor-in-Chief for IEEE Transactions on CAD. Chuck chaired the ISPD and Tau conferences and is serving as general chair for DAC 2016 in Austin.
2B - Keep Austin Wired: Routing and Clocking

Time: 1:30pm - 3:30pm | Room: Dover's

Moderator:
Jia Wang - Illinois Institute of Technology

Keeping Austin Wired is easy! But keeping modern VLSI chips wired with performance and power budgets is hard. In this session, new efforts for wiring chips will be presented. The first paper presents a framework that handles the performance constraints in global routing. The second one discusses how to improve performance by layer re-assignment. The third paper proposes parallel algorithms to speed up FPGA routing. The final paper presents a technique to synthesize clock spines for high performance designs.

2B.1 Global Routing with Inherent Static Timing Constraints
Stephan Held, Dirk Müller, Daniel Rotter, Vera Traub, Jens Vygen - Univ. of Bonn

2B.2 TILA: Timing-Driven Incremental Layer Assignment
Bei Yu - Chinese Univ. of Hong Kong
Derong Liu - Univ. of Texas at Austin
Salim Chowdhury - Oracle Corporation
David Z. Pan - Univ. of Texas at Austin

2B.3 Accelerate FPGA Routing with Parallel Recursive Partitioning
Minghua Shen, Guojie Luo - Peking Univ.

2B.4 Synthesis for Power-Aware Clock Spines
Hyungjung Seo - Samsung Electronics Co., Ltd.
Juyeon Kim - Seoul National Univ.
Minseok Kang - Samsung Electronics Co., Ltd.
Taewhan Kim - Seoul National Univ.

2C - Hardware Based Authentication

Time: 1:30pm - 3:30pm | Room: Phoenix South

Moderator:
Bao Liu - Univ. of Texas at San Antonio

This session presents novel techniques for hardware authentication. Specifically, Paper 1 replaces ECC, typically used along PUFs for authentication, with a novel fault tolerance algorithm based on ring weights. Paper 2 exploits the unique features of emerging resistive RAM technology for user password authentication. Paper 3 presents an on-chip aging sensor based on electromigration to detect recycled ICs. Finally, Paper 4 embeds capacitors in the internal layer of a printed circuit board in order to verify its authenticity.

2C.1 A Novel Way to Authenticate Untrusted Integrated Circuits
Wei Yan, John Chandy, Fatemeh Tehranipoor - Univ. of Connecticut

2C.2 RRAM Based Lightweight User Authentication
Md Tanvir Araf, Gang Qu - Univ. of Maryland

2C.3 EM-Based on-Chip Aging Sensor for Detection and Prevention of Counterfeit and Recycled ICs
Kai He, Xin Huang, Sheldon X.-D. Tan - Univ. of California, Riverside

2C.4 BoardPUF: Physical Unclonable Functions for Printed Circuit Board Authentication
Lingxiao Wei, Chaosheng Song, Yannan Liu, Jie Zhang, Feng Yuan, Qiang Xu - Chinese Univ. of Hong Kong
Special Session 2D - Dennard Scaling is History and Moore’s Law is Aging: How to Break the Inevitable Power Wall?
Time: 1:30pm - 3:30pm | Room: Austin

Moderator:
Sachin S. Sapatnekar - Univ. of Minnesota

Organizer:
Paul Bogdan - Univ. of Southern California

The relentless increase in integration densities is paving the way for full system on-chip integration and widespread adoption of multi-/manycore chips in several application domains. From consumer multimedia to high-end applications (security, healthcare, big data, etc.), new designs containing a large number of embedded cores are emerging, but potential showstoppers include challenges related to power/energy and thermal efficiencies. For a dependable manycore system, power/energy efficiency is of utmost concern due to cost, performance, scalability, and environmental impact. Moreover, increased power densities can raise on-chip temperatures, which in turn can decrease chip reliability and performance, and increase cooling costs.

Given the current trends in terms of power and performance, it is not practical to follow existing methodologies to design tomorrow’s thousand-core platforms. Consequently, new, out-of-the-box approaches need to be explored. In this special session, we will describe new, far-reaching power-efficient techniques that achieve the most sought after feature in massively integrated single-chip manycore computing platforms.

2D.1 Fine-Grain Power Management in Manycore Processor and System-on-Chip (SoC) Designs
Vivek De - Intel Corp.

2D.2 The (Low) Power of Less Wiring: Enabling Energy Efficiency in Many-Core Platforms Through Wireless NoC
Partha Pande, Ryan Gary Kim - Washington State Univ.
Zhuo Chen - Carnegie Mellon Univ.
Wonje Choi - Washington State Univ.
Diana Marculescu, Radu Marculescu - Carnegie Mellon Univ.

Paul Bogdan, Yuankun Xue - Univ. of Southern California

2D.4 Mitigating the Power Density and Temperature Problems in the Nano-Era
Muhammad Shafique, Jörg Henkel - Karlsruhe Institute of Technology

2D.5 Power and Microarchitecture Tradeoffs in Next-Generation Manycores: From Homogenous to Heterogeneous Cores and Everything in Between
Partha Kundu - Broadcom Corp.

3A - Design Automation for Non-Traditional Architectures
Time: 4:00pm - 5:30pm | Room: Phoenix North

Moderator:
Iris Bahar - Brown Univ.

Non-traditional design and architecture have been widely explored for smaller density, higher speed and lower energy consumption. Challenges for non-traditional architecture and new CAD methodologies will be presented in this session. It starts with a stochastic circuit optimization methodology for accuracy and energy tradeoffs. The second presentation talks about an analytic model to estimate the power and performance of cellular neural network. A case study is conducted to compare the CNN design based on emerging non-linear TFET solution and conventional linear resistor based design. In the last paper, the non-ideal synaptic device characteristics and the impact on on-chip learning will be studied.

3A.1 Optimizing Stochastic Circuits for Accuracy-Energy Tradeoffs
Armin Alaghi - Univ. of Michigan
Wei-Ting J. Chan - Univ. of California at San Diego
John P. Hayes - Univ. of Michigan
Andrew B. Kahng, Jiajia Li - Univ. of California at San Diego

3A.2 Analytically Modeling Power and Performance of a CNN System
Indranil Palit, Qiuwen Lou, Nicholas Acampora, Joseph Nahas, Michael Niemier, X. Sharon Hu - Univ. of Notre Dame

3A.3 Mitigating Effects of Non-ideal Synaptic Device Characteristics for On-chip Learning
Pai-Yu Chen - Arizona State Univ.
Binbin Lin - Univ. of Michigan
I-Ting Wang, Tuo-Hung Hou - National Chiao Tung Univ.
Jieping Ye - Univ. of Michigan
Sarma Vrudhula, Jae-sun Seo, Yu Cao, Shimeng Yu - Arizona State Univ.
3B - Modeling, Optimization, and Synthesis of Cyberphysical Systems

**Time:** 4:00pm - 5:30pm | **Room:** Dover's

**Moderator:**
Eli Bozorgzadeh - Univ. of California, Irvine

This session introduces design frameworks that address modeling, optimization, and synthesis of cyberphysical systems. The target applications include wearable brain machine interface, chance-constrained control systems, and aircraft environment control systems. The first paper presents methodologies for synthesizing wearable brain-machine interface. The second paper introduces an approach for chance-constrained optimization through simulations. The third paper introduces discrete-continuous optimization for cyberphysical system architecture exploration.

3B.1 Robust Communication with IoT Devices using Wearable Brain Machine Interfaces
Md Muztoba, Ujjwal Gupta, Tanvir Mustofa, Umit Y. Ogras - Arizona State Univ.

3B.2 Simulation-Guided Parameter Synthesis for Chance-Constrained Optimization of Control Systems
Yan Zhang - National Univ. of Singapore
Sriram Sankaranarayanan - Univ. of Colorado
Benjamin Gyori - Harvard Univ.

3B.3 A Mixed Discrete-Continuous Optimization Scheme for Cyber-Physical System Architecture Exploration
John Finn, Pierluigi Nuzzo, Alberto Sangiovanni-Vincentelli - Univ. of California, Berkeley

3C - The Art of Engineering Heterogeneous Computing Systems

**Time:** 4:00pm - 5:30pm | **Room:** Phoenix South

**Moderator:**
Peter Hofstee - IBM Research - Austin

Heterogeneous computing promises to be a means for more efficient computing. By leveraging the best characteristics of different compute mediums such as CPUs, GPUs, and FPGAS, it enables the exploration of multiple design goals, such as low energy consumption, high performance, etc. In this session, we will examine three exciting application spaces which have successfully been accelerated by exploiting various heterogeneous approaches.

3C.1 A User-Centric CPU-GPU Governing Framework for 3D Games on Mobile Devices
Wei-Ming Chen, Sheng-Wei Cheng - National Taiwan Univ.
Pi-Cheng Hsiu - Academia Sinica
Tei-Wei Kuo - Academia Sinica & National Taiwan Univ.

3C.2 SAT Solving using FPGA-based Heterogeneous Computing
Jason Thong, Nicola Nicolici - McMaster Univ.

3C.3 Heterogeneous Hardware/Software Acceleration of the BWA-MEM DNA Alignment Algorithm
Nauman Ahmed - Delft Univ. of Technology
Vlad-Mihai Sima, Ernst Houtgast - Bluebee
Koen Bertels, Zaid Al-Ars - Delft Univ. of Technology
Special Session 3D - From EDA to DA: Can We Evolve Beyond Our E-Roots?

**Time:** 4:00pm - 5:30pm | **Room:** Austin

**Moderator:**
Deming Chen - Univ. of Illinois at Urbana-Champaign

**Organizers:**
Andrew B. Kahng - Univ. of California at San Diego
Farinaz Koushanfar - Rice Univ.

As we approach a 2020 "wall" of silicon, patterning, device, interconnect and cost limits, and as EDA technologies and the industry itself remain in their present "mature" state, it is now more urgent to revisit question of how the field will evolve and grow. In particular, how can the paradigms and research methodologies of EDA be leveraged for design automation (DA) in other, emerging domains? Some researchers in our community are actively contributing to DA for a variety of other fields (e.g., emerging nanotechnologies, biomedical and security). But, evolution and growth as a community requires a much more systematic, coherent effort – as well as forward-looking vision to steer by. This special session is built upon and follows up on the seeds planted by the CCC Extreme Scale Design Automation workshop series. It focuses on recent efforts to systematize knowledge, trends, metrics, and visions that can help enable the EDA community to move beyond its E-roots. The audience will learn about a new IEEE CEDA technical activity group dedicated to this subject. The session includes four 15-minute talks, covering the overview and study teams within the technical activity group, as well as a 30-minute panel summarizing the recent DA challenge at DAC'15.

**PANEL: DA Perspective Challenge @DAC’15: Summary and Vision**

**Panelists:**
- Steven P. Levitan - Univ. of Pittsburgh
- Sani Nassif - Radyalis, LLC
- Naehyuck Chang - KAIST
- Jim Huang - HP Labs
- Yiran Chen - Univ. of Pittsburgh

**3D.1 Evolving EDA Beyond its E-Roots: An Overview**
Andrew B. Kahng - Univ. of California at San Diego
Farinaz Koushanfar - Rice Univ.

**3D.2 DA Systemization of Knowledge: A Catalog of Prior Forward-Looking Initiatives**
Farinaz Koushanfar, Azalia Mirhoseini - Rice Univ.
Gang Qu - Univ. of Maryland
Zhiru Zhang - Cornell Univ.

**3D.3 Toward Metrics of Design Automation Research Impact**
Andrew B. Kahng - Univ. of California at San Diego
Mulong Luo - Univ. of California at San Diego
Gi-Joon Nam - IBM Research
Siddhartha Nath - Univ. of California at San Diego
David Z. Pan - Univ. of Texas at Austin
Gabriel Robins - Univ. of Virginia

**3D.4 DA Vision 2015: From Here to Eternity**
Miodrag Potkonjak - Univ. of California, Los Angeles
Deming Chen - Univ. of Illinois
Priyank Kalla - Univ. of Utah
Steven P. Levitan - Univ. of Pittsburgh

Networking Reception

**Time:** 5:30pm - 6:00pm | **Room:** Prefunction Foyer

Whatever your goal, Networking Receptions are the perfect venue for you to expand your network and keep you connected! Join us today to catch up with your colleagues and discuss the day’s presentations with the conference presenters. The reception is included with your conference registration fee.

Special Session 10A - TAU 2015 Contest on Incremental Timing and CPPR Analysis

**Time:** 6:00pm - 6:55pm | **Room:** Phoenix North

**Moderator:**
Jin Hu - IBM Corp.

**Organizers:**
Jin Hu - IBM Corp.
Greg Schaeffer - IBM Corp.
Vibhor Garg - Cadence Design Systems, Inc.

Among timing analysis applications, timing-driven operations are imperative for the success of optimization flows, such as placement, routing, logic synthesis, and physical synthesis. Optimization transforms change the design, and therefore have the potential to significantly affect timing information. As such, timing must be kept current to ensure slack integrity and timing closure. For reasonable turnaround and performance, the timer should only incrementally update the affected portion of the design.

The aim of the TAU 2015 Contest on Incremental Timing and CPPR Analysis is to seek novel ideas for incremental timing analysis by: (i) introducing the concept and motivating the importance of incremental timing analysis and incremental common path pessimism removal (CPPR), (ii) encourage novel parallelization techniques (including multi-threading), and (iii) facilitating the creation of an incremental timing analysis framework with benchmarks to further advance this research area. This session highlights the ideas and practices of the top-performing teams of the TAU 2015 Contest.

**10A.1 TAU 2015 Contest on Incremental Timing Analysis**
Jin Hu, Greg Schaeffer - IBM Corp.
Vibhor Garg - Cadence Design Systems, Inc.

**10A.2 iTimerC 2.0: Fast Incremental Timing and CPPR Analysis**

**10A.3 OpenTimer: A High-Performance Timing Analysis Tool**
Tsung-Wei Huang, Martin D. F. Wong - Univ. of Illinois at Urbana-Champaign

**10A.4 iTRACE: A Memory Efficient Engine for Fast Incremental Timing Analysis and Clock Pessimism Removal**
Chaitanya Peddawad, Aman Goel, Dheeraj B, Nitin Chandrachoodan - Indian Institute of Technology Madras

All speakers are denoted in bold  |  * denotes Best Paper Candidate
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Special Session 10D - Rebooting Computing and Low Power Image Recognition Challenge

*Time: 6:00pm - 7:30pm | Room: Austin*

**Moderator:**
Yung-Hsiang Lu - Purdue Univ.

**Organizer:**
Yung-Hsiang Lu - Purdue Univ.

"Rebooting Computing" (RC) is an effort in the IEEE to rethink future research of computers. RC started in 2012 by the co-chairs, Elie Track (IEEE Council on Superconductivity) and Tom Conte (Computer Society). RC takes a holistic approach, considering revolutionary as well as evolutionary solutions needed to advance computer technologies. Three summits have been held in 2013 and 2014, discussing different technologies, from emerging devices to user interface, from security to energy efficiency, from neuromorphic to reversible computing. The first part of this special session introduces RC to the CAD community and solicits revolutionary ideas from the community for the directions of future computer research.

Energy efficiency is identified as one of the most important challenges in future computer technologies. The importance of energy efficiency spans from miniature embedded sensors to wearable computers, from individual desktops to mega-Watt data centers. To gauge the state of the art, the RC Committee organized the first Low Power Image Recognition Challenge (LPIRC) on June 7, 2015 in San Francisco. Each image contains one or multiple objects, among 200 categories. A participant has to provide a system that can recognize the objects and report the bounding boxes of the objects. The second part of this special session explains LPIRC and the top two winners will present their solutions.

10D.1 Rebooting Computing

*Thomas M. Conte - IEEE & Georgia Institute of Technology*
*Erik P. DeBenedictis - Sandia National Laboratories*
*Bichlien Hoang - IEEE*
*Alan M. Kadin - Princeton Junction*
*Yung-Hsiang Lu - Purdue Univ.*
*Elie K. Track - nVizix LLC & IEEE*

10D.2 Low Power Image Recognition Challenge

*Alexander C. Berg - Univ. of North Carolina, Chapel Hill*
*Rachit Garg - Purdue Univ.*
*Ganesh Gingade - Hughes Network Systems, LLC & Purdue Univ.*
*Wei Liu - Univ. of North Carolina, Chapel Hill*
*Yung-Hsiang Lu - Purdue Univ.*

10D.3 Pipelined Fast RCNN on Embedded GPU

*Boxun Li, Huizi Mao, Tianqi Tang, Yu Wang - Tsinghua Univ.*
*Jun Yao - Huawei Technologies Co., Ltd.*

10D.4 Object Detection Based on Fast Object Proposal and Representation

*Yongzhen Huang, Jingyu Liu, Junran Peng, Jingaiu Wang - Institute of Automation, Chinese Academy of Sciences*
*Tao Wang, Jun Yao - Huawei Technologies Co., Ltd.*

Special Session 10B - 2015 CAD Contest

*Time: 7:05pm - 8:30pm | Room: Phoenix North*

**Moderators:**
Natarajan Viswanathan - IBM Corp.
Shih-Hsu Huang - Chung Yuan Christian Univ.

**Organizer:**
Natarajan Viswanathan - IBM Corp.

The CAD contests at ICCAD and associated benchmark suites have been instrumental in advancing the state-of-the-art in EDA. Additionally, they have fostered productive industry-academia collaboration. In its fourth year, the 2015 CAD contest is among the largest worldwide EDA contests, attracting 112 teams from 12 regions/countries. This year’s contest is a challenging, multi-month, research and development competition, focusing on advanced, real-world problems in the three areas of system level design, logic synthesis & verification, and physical design.

This special session presents the three contest problems, releases the associated benchmarks, and announces the winners. The session also provides a venue for the top-performing teams to showcase their key ideas via short video presentations.

10B.1 Overview of the 2015 CAD contest at ICCAD

*Natarajan Viswanathan - IBM Corp.*
*Shih-Hsu Huang - Chung Yuan Christian Univ.*
*Rung-Bin Lin - Yuan Ze Univ.*
*Myung-Chul Kim - IBM Corp.*

10B.2 ICCAD 2015 Contest in 3D Interlayer Cooling Optimized Network

*Arvind Sridhar - IBM Research - Zurich*
*Mohamed M. Sabry - Stanford Univ.*
*David Atienza - École Polytechnique Fédérale de Lausanne*

10B.3 ICCAD-2015 CAD Contest in Large-scale Equivalence Checking and Function Correction and Benchmark Suite

*Chih-Jen Hsu, Chi-An Wu - Cadence Taiwan, Inc.*
*Wei-Hsun Lin, Kei-Yong Khoo - Cadence Design Systems, Inc.*

10B.4 ICCAD-2015 CAD Contest in Incremental Timing-driven Placement and Benchmark Suite

*Myung-Chul Kim - IBM Corp.*
*Jin Hu - IBM Corp.*
*Jiajia Li - Univ. of California at San Diego*
*Natarajan Viswanathan - IBM Corp.*

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