Workshop Program

2014 Int’l Workshop on Design Automation for Analog and Mixed-Signal Circuits
Thursday, November 6, 2014; colocated with IEEE/ACM ICCAD
Website: http://users.ece.cmu.edu/~xinli/2014_ams/

8am  Opening remarks: Helmut Graeb

Session 1: Design verification and test
Moderator: Yu Wang, Tsinghua Univ.

8:05am  Invited Talk: Towards Self-Learning AMS/RF Circuits and Systems: Adapting to Increasing Uncertainties in Real-Time Operating Conditions
Abhijit Chatterjee, Georgia Institute of Technology

8:50am  Poster presentations
Moderator: Helmut Graeb, Techn. Univ. Munich

NICSLU: An Adaptive Sparse Solver for Circuit Simulation
Xiaoming Chen, Yu Wang, Huazhong Yang, Tsinghua University, Beijing

A Performance-Guided Graph Sparsification Approach to Scalable and Robust SPICE-Accurate Integrated Circuit Simulations
Xueqian Zhao, Lengfei Han, Zhuo Feng, Michigan Technological University

A Unifying and Robust Method for Efficient Envelope-Following Simulation of PWM/PFM DC-DC Converters
Yo Wang, Peng Li, Suming Lai, Texas A&M University

A Zonotoped Reachability Verification for High-speed I/O Links
Ni Leibin, Sai Manoj P D, Yang Song, Hao Yu, Nanyang Technological University, Singapore

A New Optimization Algorithm for Compressing Post-Si Analog Functional Tests for Time-efficient and Cost-effective Testing
Seyed-Nematollah Ahmadyan, Shobha Vasudevan, Univ. of Illinois Urbana-Champaign

Manzil Zaheer, Xin Li, Carnegie Mellon Univ.
Chenjie Gu, Intel Corp.

Fast Statistical Analysis of Rare Circuit Failure Events via Subset Simulation in High-Dimensional Variation Space
Shupeng Sun, Xin Li, Carnegie Mellon Univ.

Reduction and IR-drop Compensations Techniques for Reliable Neuromorphic Computing Systems
Beiye Liu, Hai Li, Yiran Chen, Univ. Pittsburgh
Analog Circuit Design Knowledge Mining: Discovering Topological Similarities and Uncovering Design Reasoning Strategies

Fanshu Jiao, Sergio Montano, Christian Ferent, Alex Doboli, State University of New York Simona Doboli, Hofstra University

A Study on the Possibility of Flexible Analog Layout Migration

Po-Cheng Pan, Hung Ming Chen, National Chiao Tung Univ., Hsinchu

9:30am Posters & Coffee

Session 1 (cont'd): Design verification and test
Moderator: Sheldon Tan, UC Riverside

10am Invited Talk: ABCD and BEE: Tools for Analog/Mixed-Signal Verification via Boolean Modelling
Aadithya V Karthik, Univ. of California, Berkeley

10:45am AMS Verification using COHO-REACH
Chao Yan (Synopsys), Jije Wie (Google), Mark Greenstreet (Univ. British Columbia)

11am Design Methodologies and Verification of 3D Mixed-signal ICs
Wulong Liu, Yu Wang, Huazhong Yang, Tsinghua Univ., Beijing
Guoqing Chen, AMD Research, Beijing

Session 2: Statistical and circuit design
Moderator: Mark Greenstreet, Univ. British Columbia

11:15am Invited Talk: Synthesis-friendly High-speed I/O Architectures
Bryan Casper, Intel Corp.

12pm High-Dimensional Hierarchical Uncertainty Quantification for MEMS/IC Co-Design
Zheng Zhang, Luca Daniel, Massachusetts Institute of Technology

12:15pm Poster & Lunch

Session 2 (cont'd): Statistical and circuit design
Moderator: Ibrahim Elfadel, Masdar Institute, Abu Dhabi

1:15pm Invited Talk: Analyzing the Effects of Process Variation and Mismatch on Circuit Design: Monte Carlo and Alternatives
Michael Pronath, MunEDA GmbH

Session 3: Constraints and layout design
Moderator: Ngai Wong, Univ. of Hong Kong

2pm Invited Talk: Data structures for analog placement
*Martin D. F. Wong, Univ. Illinois at Urbana-Champaign*

2:45pm Analog Structure Tree for Floorplanning
*Shigetoshi Nakatake, Univ. Kitakyushu, Japan*

3pm Design automation of layout modules for industrial analog mixed-signal applications
*Federico Mantovani, Andreas Mueller, Infineon Technologies GA, Munich-Neubiberg*

3:15pm Posters & Coffee

**Session 4: Analog benchmarks reloaded**
Moderator: Goeran Jerke, Bosch, Germany

3:45pm Benchmarks for Analog/Mixed-Signal Macromodeling Research
*Shuqi Zhang, Ngai Wong, Univ. of Hong Kong*
*Chenjie Gu, Intel Corp.*

4pm Evaluation of a Benchmark Suite for Formal Verification of Analog Circuits
*Lars Hedrich, Felix Salfelder, Goethe Univ. Frankfurt/Main*

**Panel:**
Moderator: Xin Li, Carnegie Mellon Univ.

4:15pm Analog and Mixed-Signal IP: What Does it Take?
Panelists:
*Srinivas Modekurti, Principal Engineer, Intel Corp.*
*Bob Salem, Director of Product Marketing, Cadence Design Systems*
*Navraj Nandra, Senior Marketing Director, Synopsys*
*Ahmed Ramadan, Engineering Manager, Mentor Graphics*

4:55pm Closing remarks: Helmut Graeb

5:00pm End of workshop