REALISTIC METHOD OF 193 nm LITHOGRAPHY EXTENSIONS TO 1x-nm NODES

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ABSTRACT
The current state-of-the-art development technology in immersion lithography has successfully demonstrated resolutions down to 11 nm half pitch utilizing double or multiple patterning techniques (DPT or MPT). Even at these small feature sizes, the quality of the line edge roughness (LER) is observed excellent and within acceptable limits. The remaining challenges in applying MPT to 1x nm nodes are to have a realistic methodology for production worthy quality and quantity under acceptable cost.

Complementary lithography (or line cutting lithography) proposed by Intel utilizes the spacer quadrupling (sidewall method) to have the base grating patterns using 193-nm exposure tools. An additional step applying cutting lithography is usually done by optical or other lithographic means. Although this method requires unidirectional constraints to the IC design, the probability of success for lithography and patterning is very high.

Fabrication of the 1x-nm node using 193-nm exposure tools tends to place more stringent requirements on the overall exposure system. Not only is a very high accuracy needed in overlay and CDU at production process conditions, this is required at productivity levels that exceed normal single exposure conditions.

BIOGRAPHY
Soichi Owa is a Nikon Fellow and leading a research team on future lithography technologies. He received his Ph.D. in physics in 1987 from the University of Tokyo. He joined Nikon Corporation in 1994, where he has been engaged in the development of leading edge exposure tools for 157nm and 193nm immersion lithography. Since 2002, he has published technical papers successfully demonstrating the feasibility of water-based immersion lithography. He is a SPIE Fellow and is serving as a program committee member of SPIE Advance Lithography and International Symposium on Lithography Extensions.
DOUBLE PATTERNING: THE GOOD THE BAD AND THE UGLY. AN EDA PERSPECTIVE.

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ABSTRACT
Double patterning technologies have jumped from development groups to manufacturing teams for most sub 22nm processes. The introduction of such techniques has not been without challenges. However most of the minimum infrastructure has been put in place in time to allow design teams timely development of sub 22nm products.

Yet, there are several areas of improvement that remain to be investigated and optimized. This talk addresses the minimum infrastructure needed to design a double patterning compliant design, as well as the most common challenges that design teams face when trying to implement such techniques.

Data pertaining as to how design styles have been evolving and have facilitated the adoption of double patterning techniques will also be presented, as well as a look ahead of possible technologies that could be used to further reduce the number of iterations between physical design and manufacturing compliance checks.

BIOGRAPHY
Andres Torres holds a B.S. in Chemical Engineering from the National Autonomous University of Mexico, a M.S. in Chemical Engineering from UW-Madison and a PhD degree in Electrical Engineering from the Oregon Graduate Institute. He has been investigating the interactions between manufacturing process and electronic design flows to exploit areas of design and process co-optimization that provide more predictable and manufacturable designs. He has been with Mentor Graphics’ Design-to-silicon division since 2001 working in the areas of Resolution Enhancement Technologies, Design for Manufacturing and Process Hardening Layout Techniques. He has published over fifty papers and holds five patents in the area of semiconductor manufacturing. He is currently the Product Lead Engineer of the Litho Friendly Design group in the Design to Silicon Division.
MULTIPLE-PATTERNING OPTIMIZATIONS FOR THE LONG RUN

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ABSTRACT
Multiple-patterning lithography (MPL) has the potential to be a multi-node solution for both FEOL and BEOL patterning. MPL may also have relevance in future EUV contexts. Multiple patterning steps give rise to a number of graph coloring-centric optimizations such as pattern splitting and mask coloring assignment. Multi-modal distributions of variation have implications for characterization flows and signoff analyses. Throughout the design enablement stack – from design rule definition, to cell library design, to automatic place-and-route, to performance margins for signoff – MPL brings the specter of disruption.

Thus far, MPL enablement has naturally been biased toward “transparency” and “expediency”: flexible (“LELE”) design rules have carried the day in 20nm BEOL; cell library design still imposes relatively few demands for substantial new intelligence in placers and routers; etc. The question is whether short-term “transparency” and “expediency” will have left too much on the table, should MPL turn out to be a long-term, multi-node technology. In this talk, I will suggest some directions to investigate for recovery of missed value from MPL patterning technology in a multi-node future.

BIOGRAPHY
Andrew B. Kahng is Professor of CSE and ECE at UC San Diego. He was visiting scientist at Cadence (1995-1997) and founder/CTO at Blaze DFM (2004-2006). He has coauthored 3 books and over 350 journal and conference papers, holds 18 issued U.S. patents, and is an IEEE Fellow. He has served as international chair and co-chair of the Design working group of the International Technology Roadmap for Semiconductors since 2000. His research has developed methods for automated phase-shift mask layout, variability-aware analyses and optimizations, CMP fill synthesis, and parametric yield-driven, cost-driven methodologies for chip implementation.
**MULTIPLE E-BEAM MASKLESS LITHOGRAPHY AND IMPLICATIONS ON PROCESS, DESIGN AND CAD TOOLS**

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**ABSTRACT**
The steeply increasing price and difficulty of the mask technology make the multiple e-beam maskless lithography (MEBML2) a more preferable solution than the mask-based optical lithography, such as double patterning by using ArF immersion lithography and extreme ultra-violet lithography when going beyond the 32-nm half-pitch (HP) node. Electron beam direct writing provides extremely high resolution without jeopardy from masks, but the low productivity of traditional single beam systems makes it unacceptable for mass manufacturing even after over 3 decades of development. Considering production efficiency, the throughput of lithography tools should be in the order of 10 wafers per hour (WPH) per square meter of floor space as compared to that of an ArF scanner. Several groups have proposed different MEBML2 approaches, by multiplying either Gaussian beams, variable shape beams or character projections, to drastically increase the throughput. The maturing MEMS technology and electronic control technology enable precise control of more than ten thousands or even millions of electron beamlets, writing in parallel. Without the mask constraint, the exposure can be made by continuously scanning across the entire wafer diameter as long as the ultra-high speed data rate can be supported. Hence a much slower scan speed is required and therefore a small tool footprint is achievable.

The MAPPER Pre-Alpha Tool, composed of a 110-beam 5-keV column and a 300-mm wafer stage within a vacuum chamber of 1.3x1.3m² footprint, has been installed and operational for process development in the advanced Giga-Fab cleanroom environment. By sending the pre-treated optical data to the corresponding photodiode of each blanker, each beam writes its own features independently in raster scan mode. Resolution beyond 30-nm HP resolution for both C/H and L/S by using chemical amplified resist has been demonstrated. Applying proper e-beam proximity corrections (EPC), the 20-nm node test circuit layout has been successfully patterned. The future upgrade by a new electron-optics column, containing more than 10-thousands beamlets and each beamlet projecting 7x7 sub-beams, will achieve throughput at 10 WPH of 32-nm HP node wafers by a single chamber, and 100WPH by clustering 10 chambers.

If the productive MEBML2 carries out, it will greatly change the concepts of lithography process and design from the current double patterning for 32nm HP and beyond nodes. First, the cycle time will be largely reduced by saving mask making and reducing double patterning to single patterning for all critical layers. It has the opportunity of quickly modifying the EPC model or even directly correcting vulnerable layout hotspots when found, without the headache of retooling the expensive mask. Then owing to its high resolution, the restricted design rules due to the limitation of optical lithography or double patterning will be removed. But some new rules may be added in considerations of the writing approaches and the stitching effect among the massive beams, which may not be avoided and needs some smart ways to take good care of. The extremely high data rate, >10TB per second, requires new file format and hardware specification of the data path inside the tool. The off-line data preparation such as logic operation and EPC may become bottleneck if keeping nowadays speed. Accelerated computing solutions by software and hardware are essential.
Figure 1 The resolution test of the MAPPER Pre-Alpha tool with 25-nm spot size using CAR resist. Ignoring the resist collapse at 26- and 24-nm HP line/space, the ultimate resolution at 22-nm HP for both CH and LS has marginally been demonstrated. Further shrinking the beam size can readily resolve these pitches and even resolve smaller pitches.

REFERENCES

BIOGRAPHY
Jack J.H. Chen, is currently the manager of the Maskless Lithography Program in TSMC. He joined the company as a lithographer since 1995 when he received the master degree of Physics from National Taiwan University. After successfully promoting the immersion ArF lithography into production line in 2007, he was assigned to take the lead on this program. By evaluating several Multiple E-beam Direct Writing solutions in the world, his team has focused on the MAPPER technology which is the only low (5) keV solution and believed the most feasible one to achieve the 10-WPH throughput per single EO column in a reasonable cost.
E-Beam Direct Write (EBDW) Options for Sub-20 nm Lithography: Multiple Technology Choices and the Impact on Design

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ABSTRACT
The trend to constantly shrinking device geometries embodied by Moore’s Law is well known throughout the industry. In recent years, the explosion in development and manufacturing costs with decreasing geometry size has become equally well known. For the newest lithography options below 20 nm it has been suggested that the true limitations facing the industry are economic, not technological: we can build them, but can we afford them?

One key component in any cost analysis, especially for Extreme Ultra-Violet (EUV) or multiple exposures using 193 nm immersion, is the cost of the masks, not just the actual masks used to produce volume products but also the hundreds of critical masks that are consumed in research, process development, device prototyping and re-spins required for various reasons. Maskless technologies such as EBDW have often been proposed as a cost-effective alternative to the most expensive mask based options, but the painful truth is that the throughput of the best EBDW tools today is measured in wafers per day, not the many tens of wafers per hour (WPH) required for volume production. Over the years many suppliers have proposed faster EBDW tools, typically based on arrays of thousands of electron beams writing simultaneously. The leading candidates have even produced pre-alpha tools which are currently generating valuable learning. While promising, none of these options is ready for production yet.

Other EBDW options have also been discussed, ranging from just a few wafers per hour to replace the large number of non-production reticles, to low tens of WPH tools to augment mask based technologies for specific patterns. One option worth discussing is printing perfect arrays of one-dimensional lines and spaces with a conventional exposure tool, possibly enhanced through self-aligned double patterning (SADP) or directed self-assembly (DSA), then using the e-beam tool simply to cut the lines. This approach can enable greatly increased throughput on EBDW tools with specific architectures, and could also be used to print contact layers at reasonable speeds.

In this paper we will consider the tradeoffs between the various EBDW options under consideration, and discuss how these options impact design and layout – and how EBDW aware design can greatly accelerate the adoption of these cost containment options.
BIOGRAPHY

Moshe Preil is the manager of Emerging Lithography and Tools, part of the Strategic Lithography Technology department at GLOBALFOUNDRIES. His group is tasked with exploring all potential tool options to extend lithography below the 14 nm node, as well as investigating strategic questions related to the 20 and 14 nm nodes currently in development.

Prior to joining GLOBALFOUNDRIES he spent 15 years on the supplier side of the industry working in various lithography, process control and yield management positions, including reticle inspection, overlay and CD metrology and control, yield enhancement consulting, and advanced lithography strategies. For the preceding 12 years he was a lithography engineer at several companies, mainly AMD and Sierra Semiconductor (whose fab was an early stage predecessor to Chartered Semiconductor). His primary work in the fab involved implementing leading edge steppers and scanners for both advanced development as well as production. In his previous position at AMD he was involved in the early development of deep-UV technology. He has also been active in the Sematech lithography community, and was a member of the early 193 nm steering committee at Sematech.

Dr. Preil earned his PhD in physics from the University of Pennsylvania working on optical and electron spectroscopies of novel graphite based compounds. He has published numerous journal papers, been issued 9 United States patents, and was the co-editor of the recent JM3 special issue on metrology.
E-beam Direct-Write and EDA

Lars Bomholt
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ABSTRACT
The high resolution of E-beam lithography makes it one of the contenders at the leading edge of deep submicron lithography. Various companies are developing tools that overcome the issue of scaling e-beam direct-write lithography to the high-volume demands of mass production. What does it mean to EDA (electronic design automation)?

EDA’s primary objective is the creation of the designs that are transferred to the wafer. EDA also provides tools for process development, device characterization, as well as tools that correct for inadequacies of the manufacturing process and prepare the data for the lithography equipment. New lithographic technologies create challenges and opportunities in all of those areas.

This talk gives an overview of the impact of e-beam direct-write lithography on EDA. The primary focus is on the infrastructure for proximity correction and data preparation, but it also touches upon related issues, such as process modeling and the impact on design.

BIOGRAPHY
Lars Bomholt is technologist in the Silicon Engineering Group at Synopsys. His focus is semiconductor technology modeling and tools for computer-aided manufacturing. He holds a PhD in technical sciences from the Swiss Federal Institute of Technology, Zurich.
EUV Lithography – Prospects and Challenges

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ABSTRACT
ArF lithography uses 193nm illumination to project the image of a mask containing circuit patterns onto the wafer. It has been the mainstay of leading-edge integrated circuit manufacturing technologies for several process generations. However, now the feature size and pitches that are required to be defined to continue Moore’s Law scaling are proving to be outside the reach of conventional ArF lithography.

In response, two leading approaches have been developed by lithographers: a) extension of ArF lithography through the use of process tricks like double patterning, and b) using EUV lithography with a lower wavelength of 13.5nm. Both approaches have their advantages and limitations and are the subject of intense research and development currently.

EUV lithography brings several powerful advantages to the table – it greatly simplifies layout and has the potential for simplifying design rules and limitations related to Optical Proximity Correction. It eliminates or reduces a lot of the complications that double patterning causes including layout restrictions and drawing layers required to represent the desired layout. However, the physics and chemistry of EUV lithography introduces several new concerns especially related to CD variability that are of great interest to the device and circuit designer. Moreover, EUV lithography has formidable practical engineering challenges for high volume manufacturing that are still being worked on.

ArF double patterning and EUV lithography present two drastically different options for meeting the scaling needs of future process technologies. They drive dramatically different choices in design rules, patterning tradeoffs and impacts to device architecture, circuit design and layout. It is crucial for the device and circuit designer to understand what these upcoming technologies bring to the table so that in concert with the lithographer, they can make the right decisions to accommodate their advantages and disadvantages into the chip planning cycle appropriately.

In this paper, the current status of EUV lithography will be examined, as well as the key advantages and disadvantages of the technique from the point of view of the device, circuit and layout.

BIOGRAPHY
Sam Sivakumar is an Intel Fellow and Director of Lithography in Intel's Portland Technology Development Group in Oregon. He is responsible for the definition, development and deployment of Intel's next generation lithography processes, resolution enhancement techniques and optical proximity correction.

Sam joined Intel in 1990 after graduating from the University of Illinois at Urbana-Champaign and throughout his career with the company has worked in the lithography area on photoresists, patterning equipment and process development. He has contributed to lithography development, characterization and transfer to high-volume manufacturing of every submicron process technology generation at Intel since 1990.
A FOUNDRY PERSPECTIVE ON EUV LITHOGRAPHY

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ABSTRACT
The limited extensibility of double patterning, along with design challenges and significant increases to mask set costs and cycle time, provide foundries with motivations to consider alternative lithographic technologies. One such alternative with substantial potential for extensibility is EUV lithography. Significant improvements in EUV source power will be required to bring EUV lithography costs below those of double patterning. Many other aspects of EUV lithographic technology, such as equipment reliability and stability, need to mature for effective use of EUV lithography in manufacturing. EUV resists will have adequate performance for initial use in logic, but will require improvement for later nodes. EUV mask making and handling, particular concerns for foundries, also need improvement. Fully exploiting the resolution potential of EUV lithography will require commensurate advances in metrology.

BIOGRAPHY
Harry J. Levinson is Sr. Fellow and manager of GLOBALFOUNDRIES’ Strategic Lithography Technology Department, which is responsible for advanced lithographic processes and equipment. Dr. Levinson started his career at AMD, then spent some time at Sierra Semiconductor and IBM, before returning to AMD – now GLOBALFOUNDRIES – in 1994. He has published numerous articles on lithographic science and is the author of two books, Lithography Process Control and Principles of Lithography. He holds nearly 50 US patents. He has a BS in engineering from Cornell University and a PhD in Physics from the University of Pennsylvania.
EUV PATTERN CORRECTION FOR 56 NM METAL PITCH

Martin Burkhardt
IBM

ABSTRACT
For the logic generations of the 15 nm node and beyond, the printing of pitches around 56 nm are needed. For EUV lithography to replace ArF-based multi-exposure techniques, it is required to print these patterns in a single exposure process. The most aggressive pitch is likely to be found on the lower metallization levels. We introduce basic imaging needs for this device generation and use an experiment of a straight shrink of a 22 nm circuit as an example.

The \( k_1 \) factor is roughly 0.6 for 64 nm pitch at an NA of 0.25, and \( k_1 \sim 0.52 \) for 56 nm pitch. These \( k_1 \) numbers are of the same order at which model based OPC was introduced in KrF and ArF lithography a decade or so earlier. In previous work for the 22 nm node test devices using EUV we used a simple threshold OPC model without further resist model calibration. For 64 nm pitch at an NA of 0.25, the OPC becomes more important, and at 56nm pitch OPC becomes necessary. For 15nm node lithography, we resort to a full resist model calibration using tools that were adapted from conventional optical lithography. We use a straight shrink 22nm test layout to assess post-OPC printability of a metal layer at pitches at 64nm and 56nm, and we use this information to correct test layouts.

BIOGRAPHY
After working on x-ray lithography at MIT, Martin Burkhardt joined Texas Instruments in 1995, where he worked on optical proximity correction and lithography simulations. From 1998 to 2001 he worked on lens aberrations and simulations at ASML in Veldhoven, before joining IBM in 2001. He has since worked on OPC and resolution enhancement techniques for advanced lithography nodes, most recently at EUV wavelengths.
EUV Lithography for 1X nm Device Manufacturing

William H Arnold

Abstract
EUVL lithography using high resolution step and scan systems operating at 13.5nm is being inserted in leading edge production lines for memory and logic devices. These tools use mirror optics and either laser produced plasma (LPP) or discharge produced plasma (DPP) sources along with reflective reduction masks to image circuit features. These tools show their capability to meet the challenging device requirements for imaging and overlay. Next generation scanners with resolution and overlay capability to produce 1X nm memory and logic devices are in preparation. Challenges remain for EUVL, the principal of which are increasing source power enabling high productivity, building a volume mask business encouraging rapid learning cycles, and improving resist performance so it is capable of sub 20nm resolution.

Biography
For 14 years, Bill Arnold is the Chief Scientist of ASML. Since 2001 he is also the Vice President of ASML’s Technology Development Center. While at ASML, he has contributed to the development of KrF, ArF, ArF immersion and now EUV scanners. Before joining ASML, he worked 18 years at AMD developing lithography and etch processes for many generations of memories and processors. In 2011, Bill was elected Vice President of SPIE, the International Society for Optics and Photonics, and in 2013 he will be the Society President.