



Original technical submissions on, but not limited to, the following topics are invited:

1) SYNTHESIS, VERIFICATION AND PHYSICAL DESIGN

1.1 Logic and High-Level Synthesis:

- Synthesis, technology mapping
- Refinement techniques
- Direct compilation and post-optimization
- Micro-architectural transformations
- Memory system synthesis

1.2 Simulation and Formal Verification:

- Formal verification techniques
- HW/SW co-simulation
- Switch, logic, behavioral, and system-level simulation and validation
- Protocol and interface design for correctness
- Software verification
- Emulation
- Hybrid systems
- Post-silicon validation (for functional design errors)

1.3 Partitioning, Placement and Floorplanning:

- High-level physical design and synthesis
- Estimation and hierarchy management
- Partitioning, floor-planning and global placement
- Detailed and incremental placement

1.4 Routing and Detailed Physical Design:

- Detailed routing, including routing for yield, manufacturability, and timing
- Post-placement layout optimization.

1.5 Optimization in Physical Design:

- Optimization for area, timing, power, and yield
- Interaction between physical design and logic synthesis.

2) SYSTEM-LEVEL CAD

2.1 System Design:

- System-level specification and modeling and simulation
- System design flows and methods
- Models of computation
- HW/SW co-design, co-optimization, and co-exploration
- HW/SW platforms
- Rapid prototyping
- System design case studies and applications

2.2 Embedded Systems Hardware:

- Multi-core/multi-processors systems
- On-chip communication and networks-on-chip
- Static and dynamic reconfigurable architectures
- Regular circuits, structured ASICs
- Application-specific instruction-set processors (ASIPs)
- Memory hierarchies and management
- System-level issues for 3-D integration

2.3 Embedded Systems Software:

- Real-time software and RTOS
- Middleware
- Timing analysis and WCET
- Programming models for multi-core systems
- Profiling and compilation techniques

2.4 Power and Thermal Considerations in System Design:

- Power and thermal estimation, analysis, optimization, and management techniques for hardware and software systems

3) CAD FOR RELIABILITY, MANUFACTURABILITY, AND TEST

3.1 Design for Manufacturability:

- CAD for the design/manufacturing interface, CAD support for OPC and RET, variability analysis, yield estimation
- Manufacturable layout

3.2 Testing:

- Fault modeling, delay test, analog and mixed signal test
- Fault simulation
- ATPG, BIST and DFT
- Memory test and repair
- Technology impact on test
- Post-silicon validation and debug (for electrical, physical, and timing issues)

3.3 Design for Reliability:

- Design techniques for achieving reliability, resilience and robustness from unreliable components
- Analysis of thermal, reliability, aging, NBTI, electromigration, wearout, etc., effects in CMOS and mixed technologies and physical domains
- Reliability issues in system design and 3-D integration

4) CAD FOR CIRCUITS, DEVICES, AND INTERCONNECT

4.1 Analog, Mixed-Signal, RF and Multi-Domain Simulation:

- Numerical methods for analog, mixed-signal, RF, multi-domain (MEMS, nanoelectronic, optoelectronic, biological, etc.) network and system simulation
- Nonlinear model reduction and computational macromodeling
- Fast analysis of large-scale circuits and systems
- Computer-aided analysis, design, and simulation of electronic and mixed-domain devices including semiconductor, nanoelectronic, micromechanical, and electro-optical devices
- Compact device modeling and modeling of device variability

4.2 Analog, Mixed-Signal, RF and Multi-Domain Synthesis and Optimization:

- Advances in low power, variation-aware, high speed design methodology and tools
- Structural synthesis, sizing, design centering, symbolic and formal analysis, constraint management
- Analog place and route
- Synthesis and design methods for MEMS, electro-optical, and other mixed technology systems

4.3 Timing and Behavioral Modeling:

- Gate-, switch-, and block-level modeling
- Timing analysis and methodologies including statistical timing
- Current-source modeling
- Behavioral modeling of circuits and systems

4.4 Interconnect and Power Networks:

- Network-level power/ground and package analysis and optimization
- Reduced order modeling of interconnect and linear time invariant networks
- Signal integrity analysis
- Interconnect parameter extraction
- Electromagnetic simulation and package analysis
- EMC/EMI simulation techniques

5) CAD FOR NANOSCALE AND BIOLOGICAL SYSTEMS

5.1 Biological Systems:

- Computer-aided analysis techniques for biological systems -biomolecular, intracellular, cellular, organ and organism level
- Analysis and design of synthetic biological systems. Multi-scale biological systems, systems biology

5.2 Nanoscale and Post-CMOS Systems:

- Analysis, synthesis and design methods for novel devices (eg., quantum, molecular, spin-based) and systems centered about future nanotechnologies
- Bio-electronic devices and systems.

About ICCAD:

ICCAD serves EDA and design professionals, highlighting new challenges and innovative solutions for Integrated Circuit Design Technologies and Systems. ICCAD covers the full range of CAD topics - from device and circuit-level CAD up through system-level CAD and embedded software, as well as CAD for post-CMOS design and novel application areas, such as biology and nanotechnology.

SUBMISSION DETAILS

Paper submissions must be done through the online submission system at: <http://www.easychair.org/conferences/?conf=iccad2011>

Regular papers will be reviewed as finished papers; preliminary submissions will be at a disadvantage.

REGULAR PAPER SUBMISSIONS

All papers must be in PDF format only, with saveable text.

Each paper must be no more than 8 pages (including the abstract, figures, tables, and references), double-columned, 9pt or 10pt font.

Your submission must not include information that serves to identify the authors of the manuscript, such as name(s) or affiliation(s) of the author(s), anywhere in the manuscript, abstract, or in the embedded PDF data. References and bibliographic citations to the author(s) own published works or affiliations should be made in the third person.

Submissions not adhering to these rules, or determined to be previously published (this includes pre-prints publicly available on personal or other websites, such as arXiv, or publicly available internal memoranda with author names divulged) or simultaneously submitted to another conference, or journal, will be summarily rejected. Internal memoranda with full content not publicly available, and with author names not divulged, may be submitted.

TEMPLATES

These will be available on the ICCAD website, www.iccad.com, for your convenience, but are not required.

PROCEEDINGS

The deadline for final papers is **Friday, August 12**. Accepted papers are allowed 4 pages in the conference proceedings free of charge. Each additional page beyond 4 pages is charged \$125.00 per page. IEEE will hold the copyright for ICCAD 2011 proceedings. Authors of accepted papers must sign an IEEE copyright release form for their paper.

CONFERENCE REGISTRATION

At least one author per accepted paper must register by Monday, August 8 at the discounted speaker's registration rate. Failure to register will result in your paper being removed from the conference proceedings. IEEE reserves the right to exclude a paper from distribution after the conference (e.g., removal from IEEE Xplore) if the paper is not presented at the conference.

ACM/IEEE WILLIAM J. MCCALLA ICCAD BEST PAPER AWARD

One or more outstanding submissions will be recognized with this prestigious award.

NOTIFICATION OF ACCEPTANCE

Authors will be notified of acceptance on or before

Friday, July 1, 2011. Final paper guidelines will be sent at that time.



PROPOSALS

Call for Workshop, Tutorial, Special Session, Panel and Keynote Proposals April 29, 2011

WORKSHOP PROPOSALS

ICCAD provides a vibrant and supportive environment for small-to-medium-sized affiliated workshops. Typical workshops are one-day events on the Thursday of ICCAD, with ICCAD providing all logistical support (registration, lunch, room bookings, hotel, pre-conference financials, etc.) All workshop proposals should be sent to Joel Phillips, General Chair, at jrp@cadence.com.

TUTORIAL PROPOSALS

All ICCAD tutorials are embedded in the main technical program and free to conference attendees, providing value to attendees and a good audience for presenters. Typical tutorials run 1.5-2 hours, although longer tutorials (consisting of two session blocks of 1.5-2 hours each) may be considered. Tutorial suggestions should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants with biographical data. Proposals should focus on the state-of-the-art in a specific area of broad interest amongst ICCAD attendees. All tutorial proposals should be sent to Jörg Henkel, Tutorial Chair, at henkel@kit.edu.

SPECIAL SESSION PROPOSALS

Special Sessions are 1.5 hours. Special session proposals should focus on in-depth treatment on a topic of timely interest to the ICCAD audience. Special session proposals should not exceed two pages, should describe the topic and intended audience, and must include a list of suggested participants with biographical data. All special session proposals should be sent to Jörg Henkel, Tutorial Chair, at henkel@kit.edu.

PANEL PROPOSALS

Panel suggestions should not exceed two pages, should describe the topic and intended audience, and should include a list of suggested participants. Panel suggestions must include a bulleted outline of covered topics. All panel proposals should be sent to Helmut Graeb, Technical Program Vice-Chair at graeb@tum.de.

KEYNOTE PROPOSALS

Keynote proposals should include descriptions of suggested keynote speakers, and the importance of the speech to the ICCAD audience. All keynote proposals should be sent to Alan Hu, Technical Program Chair at ajh@cs.ubc.ca.

ICCAD reserves the right to restructure all panel, special session, and tutorial proposals.

If you need assistance, please contact the appropriate committee members:

Joel Phillips, General Chair: jrp@cadence.com

Alan Hu, Technical Program Chair: ajh@cs.ubc.ca

Helmut Graeb, Technical Program Vice-Chair: graeb@tum.de

Jörg Henkel, Tutorial Chair: henkel@kit.edu

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