

Registration - 7:00am - 6:00pm (Bayshore Foyer)
 Speakers' Breakfast - 7:30am (Monterey Room)

Tuesday, November 6, 2007

OPENING SESSION & KEYNOTE ADDRESS

The Semiconductor Industry's Nanoelectronics Research Initiative: Motivation and Challenges for Technology and Design
 Jeff Welser - Director, SRC Nanoelectronics Research Initiative, Semiconductor Research Corporation,
 IBM Almaden Research Center, San Jose, CA (Pine/Fir Ballroom)

8:30

10:00

Coffee Break sponsored by: **ALTERA**

Oak Ballroom	Fir Ballroom	Pine Ballroom	Cedar Ballroom
SESSION 1A	SESSION 1B	SESSION 1C	SESSION 1D
Advances in Parasitic Extraction & Variability Modeling	Networks-on-Chip & Latency-Insensitive Systems	Power Grid Analysis	Synthesis & Verification of Quantum Circuits

10:30

12:00

12:00pm - 1:30pm **ICCAD LUNCH PANEL: Ethics During Transitions** (Donner Ballroom)
 Organized & Supported by IEEE CEDA

SESSION 2A	SESSION 2B	SESSION 2C	SESSION 2D
Connecting Physical Challenges & Design Approaches	Analytical Techniques for Physical Optimization	Logic Synthesis	Memory Optimization & System-Level Timing

1:30

3:30

Coffee Break

SESSION 3A	SESSION 3B	SESSION 3C	SESSION 3D
Resilient & Regular Circuits	3-D Integration Challenges	Applications of SAT & QBF	Embedded Tutorial: Physical Synthesis Comes of Age

4:00

5:30

PANEL RECEPTION 5:30pm - 6:15pm (Gateway Foyer)

ICCAD IDOL PANEL • 6:15pm - 7:15pm (Pine/Fir Ballroom)

Annual ACM/SIGDA Dinner with invited speaker - Gene Amdahl 7:30pm - 9:30pm (Donner Ballroom)

Wednesday, November 7, 2007

Technology Fair: 10:00am - 4:00pm (Gateway Foyer)

Registration - 7:00am - 6:00pm (Bayshore Foyer)

Speakers' Breakfast - 7:30am (Monterey Room)

	<i>Oak Ballroom</i>	<i>Fir Ballroom</i>	<i>Pine Ballroom</i>	<i>Cedar Ballroom</i>
	SESSION 4A	SESSION 4B	SESSION 4C	SESSION 4D
8:30	High Quality Test Cases for Verification	Advances in Embedded Systems	Embedded Tutorial: Can Nano-Photonic Silicon Circuits become an INTRA-Chip Interconnect Technology?	Designers' Perspective: Memory Design Challenges in sub-65-nm Technologies
10:00	<i>Coffee Break</i>			
	SESSION 5A	SESSION 5B	SESSION 5C	SESSION 5D
10:30	Scaling Formal Verification	Advances in Statistical Timing & Optimization	Sequential Synthesis & FPGA Mapping	Designers' Perspective: High Speed I/O
12:00	<i>12:00pm - 1:00pm ICCAD Lunch "Honoring Margarida Jacome" (Donner Ballroom)</i>			
	<i>1:00pm - 1:30pm Technology Fair Dessert (served in Gateway foyer)</i>			
	SESSION 6A	SESSION 6B	SESSION 6C	SESSION 6D
1:30	Advances in Routing & Clock Design	Improving Delay Test Generation & Performance Predictors	High Level Synthesis	Analog Circuit Optimization
3:30	<i>Coffee Break</i>			
	SESSION 7A	SESSION 7B	SESSION 7C	SESSION 7D
4:00	Global Routing	Test Compression & Test Power	Gate Level Physical Synthesis	Designers' Perspective: Foundry and Circuit Designer Communication
6:00	<i>25th Anniversary Banquet</i> - SURPRISE PERFORMANCE (<i>Donner Ballroom</i>) • 7:00pm - 9:00pm			

Designers' Perspective sessions are grey.

<i>Oak Ballroom</i>	<i>Fir Ballroom</i>	<i>Pine Ballroom</i>	<i>Cedar Ballroom</i>	
SESSION 8A	SESSION 8B	SESSION 8C	SESSION 8D	8:30
Interconnect Modeling & Optimization	Embedded Tutorial: Formal Verification at Higher Levels of Abstraction	Floorplanning	System-Level Synthesis & Interconnect Design	10:00
<i>Coffee Break</i>				
SESSION 9A	SESSION 9B	SESSION 9C	SESSION 9D	10:30
Advances in Model Order Reduction Techniques for Interconnect Analysis	Embedded Tutorial: Mosfet Modeling for 45nm & Beyond	Voltage Assignment in Floorplanning	Variation Tolerant Circuits	12:00
<i>12:00pm - 1:00pm Lunch (Hotel Restaurant)</i>		<i>Keynote: Overcoming the Process Variability Crisis via Proactive DFM</i> 1:00pm - 1:45pm Oak Ballroom John Kibarian - President and CEO, PDF Solutions, Inc., San Jose, CA		
SESSION 10A	SESSION 10B	SESSION 10C	SESSION 10D	2:00
Advanced Models for Static Timing Analysis	Variation Aware Timing Verification	Reliability Driven Modeling & Analysis for Deep Submicron Technologies	Design Automation and Defect Tolerance Techniques for Emerging Technologies	4:00
<i>Coffee Break</i>				
SESSION 11A	SESSION 11B	SESSION 11C	SESSION 11D	4:30
Leakage Power Reduction	Power Modeling & Optimization	Improving Planarity & Patterning	Model Order Reduction for Parameterized & non-Linear Systems	6:30
				6:45