

## ICCAD-99 AT A GLANCE

### Full-Day Tutorials

Continental Breakfast - 8:00AM - 9:00AM (Gateway Foyer)

Tutorial Registration - 8:00AM - 10:00AM (Bayshore Foyer)

Lunch - 12:00PM - 1:00PM (Gateway Foyer)

#### THURSDAY, NOVEMBER 11

9:00 AM **TUTORIAL 1** 5:00 PM

Mixed-Signal ASIC Design: CAD,  
Methodology, Case Studies

(CEDAR BALLROOM)

9:00 AM **TUTORIAL 2** 5:00 PM

Modern Physical Design:  
Algorithm, Technology  
and Methodology

(PINE BALLROOM)

9:00 AM **TUTORIAL 3** 5:00 PM

Low Voltage/Low Power Design  
Methodologies and CAD

(FIR BALLROOM)

9:00 AM **TUTORIAL 4** 5:00 PM

Signal Integrity in High  
Performance Design

(OAK BALLROOM)

## MIXED-SIGNAL ASIC DESIGN: CAD, METHODOLOGY, CASE STUDIES

Time: 9:00 to 5:00

Room: Cedar

### Speakers:

**Rob Rutenbar** - Carnegie Mellon Univ., Pittsburgh, PA

**Georges G.E. Gielen** - Katholieke Univ. Leuven, Belgium

**Jim Holmes** - Texas Instruments, Dallas, TX

**Frank Op't Eynde** - Alcatel Microelectronics, Zaventem, Belgium

**Paolo Miliozzi** - Conexant Systems, Inc. Newport Beach, CA

**Koen Lampaert** - Conexant Systems, Inc., Newport Beach, CA

**Background:** Modern System-on-Chip (SoC) designs are increasingly mixed-signal designs. Unfortunately, just as deep submicron technologies have complicated the design of digital functions with issues such as the design of digital functions with issues such as practical complexity management and predictable timing closure, likewise these technologies complicate the analog subsystems on SoC designs. Since analog circuits exploit (rather than abstract away) the low-level physics of the fabrication process, they remain difficult and costly to design, validate, reuse. The desire to do hand-crafted, one-transistor-at-a-time analog design is increasingly at odds with the need for more analog design productivity, practical circuit synthesis and reuse, and reliable verification at all levels of the mixed-signal hierarchy.

This tutorial is about recent progress in tools and methodologies for complex mixed-signal designs. The ad hoc (and often, nonexistent) analog methodologies of the past will not suffice for the future. The tutorial focusses on emerging mixed-signal tools and technologies, including industrial case studies of some real flows and designs. The intended audience is CAD professionals responsible for implementing or maintaining analog- or mixed-signal tools or flows, and circuit / system designers who have to live with the resulting tools and flows.

**Description:** The tutorial is divided into two sessions. The morning session will overview emerging CAD ideas and methodologies for mixed-signal designs. The first section will focus on analog building blocks (e.g., amplifiers, comparators) with emphasis on circuit and physical synthesis, libraries and reuse strategies. The second section will focus on system-level, architecture-level design, with emphasis on analog behavioral modeling and power/area/noise estimation.

The afternoon session will focus on examples of industrial CAD flows and design case studies. We will discuss barriers to top-down mixed-signal design in the real world practical methodologies for complex SoC designs, industrial reuse and IP strategies and radio frequency design methodology. Case studies include data channels, a commercial ISDN chip, and a front-to-back RF IC design flow.

Our overall goal is to give the attendee a clear picture of leading-edge industrial mixed-signal design practice, and the outlook for emerging research-level tools, techniques, and methodologies.

## MODERN PHYSICAL DESIGN: ALGORITHM, TECHNOLOGY AND METHODOLOGY

Time: 9:00 to 5:00

Room: Pine

### Speakers:

**Andrew B. Kahng** - Univ. of California, Los Angeles, CA

**Majid Sarrafzadeh** - Northwestern Univ., Evanston, IL

**Background:** This tutorial will cover "the latest word" in physical chip implementation methodology and physical design (PD) algorithm technology. The target audience consists of system and circuit designers who would benefit from understanding tool capabilities in this arena, for CAD engineers (both R&D and support), for design project managers, and for academic researchers. Familiarity with basic PD methodology is assumed.

**Description:** The first section will briefly review implications for PD of the process technology and system design roadmaps. A convergent RTL-down chip planning and implementation methodology will be given as context for the ensuing material. Fundamental PD problem formulations and algorithms will be summarized, concentrating on latest developments in partitioning, block placement and top-level interconnect optimization, and cell-based place-and-route. We will motivate needs for incremental optimization techniques, dealing with incomplete design data, and new tool interactions and concurrent optimizations.

The second section will zero in on "upstream interactions", i.e., interactions between traditional PD and upstream floorplanning and logic synthesis. Various approaches to achieving a convergent, predictable implementation flow will be reviewed. These center around alternate methodologies for prediction/predictability and estimation, e.g., budgeting-based planning, small blocks + wireplanning, layout-driven logic synthesis, constant-delay, etc. Particular attention will be given to performance and signal integrity optimizations.

The third section will focus on interactions with parasitic estimation, delay calculation, and timing/power/SI validations. Specific requirements for tight analysis loops, and issues for data modeling, data flows, and database organization will be discussed.

The final section will describe new linkages between traditional PD and custom layout and polygon-level optimizations. Such linkages, which may soon permeate high-end ASIC methodologies, are the consequence of manufacturability and cost considerations (\$/wafer, catastrophic and parametric yield, sources of manufacturing variability). Process drivers for PD (e.g., phase-shifting masks and layout density control for uniform planarization) also provide strong impetus for PD to adopt custom-on-the-fly methodology.

## LOW VOLTAGE/LOW POWER DESIGN METHODOLOGIES AND CAD

Time: 9:00 to 5:00

Room: Fir

### Speakers:

**Farid N. Najm** - Univ. of Toronto, Toronto, Canada

**Anantha Chandrakasan** - Massachusetts Institute of Technology, Cambridge, MA

**Rajendran Panda** - Motorola, Inc., Austin, TX

**Background:** By way of introduction, we will first briefly review the low power/low voltage problems and provide an outline of the rest of the tutorial, which will be in three parts.

**Description:** The first part is focused on design techniques. Several emerging technologies such as Multiple and Variable threshold CMOS enable low voltage/low power high performance computing while providing a “knob” to dynamically adjust leakage currents. The challenges in design methodologies and tools for these technologies will be discussed. In many applications, there is significant energy advantage in using an embedded power supply scheme where the voltage can be adapted based on computational demand. Rather than designing a system with a static supply to meet a specific timing constraint under worst case conditions, it is more energy efficient to allow the voltage to vary such that the timing constraints are just met at any given operating condition. The key challenges will be discussed including regulator design, circuit styles and scheduling. Trends in low-voltage library design will also be discussed and will cover logic, memory and low-swing interconnect drivers.

In the second part, we will deal with issues of power estimation and modeling. Estimation and modeling are central to any low power design methodology. After an introduction to fundamentals of power estimation, we will discuss power modeling at the gate/cell level. These models allow power analysis to be done at higher than the transistor level. Modeling and estimation at even higher levels (e.g., RTL) are key to doing early design exploration. These will be discussed next, covering both bottom-up and top-down techniques.

Finally, we will cover power/ground bus analysis and design, power optimization, and leakage power estimation and optimization. An overview of the performance, signal integrity, and electromigration reliability issues related to power distribution problems will be given. Common design styles for power distribution, and a unified methodology to design, analyze, and verify large power/ground grids will be presented with case studies. Modeling of package inductance, decoupling capacitors, and circuit parasitics to study their effect on power grid design will be discussed. Techniques to reduce power grid simulation effort, such as vector compression and static determination of worst case power demand scenario will also be considered. Combinational/sequential logic restructuring, encoding and several special design techniques for power reduction will be reviewed. Some recent transistor level and gate level optimization techniques to reduce leakage power in dual-Vt circuits will also be presented.

## SIGNAL INTEGRITY IN HIGH PERFORMANCE DESIGN

Time: 9:00 to 5:00

Room: Oak

### Speakers:

**David Blaauw** - Motorola, Inc., Austin, TX

**Anirudh Devgan** - IBM Corp., Austin TX

**Abhijit Dharchoudhury** - Intel Corp., Austin, TX

**Background:** This tutorial is intended to help circuit designers, CAD tool developers, and researchers gain an understanding of the problems, available analysis tools, and mitigating circuit techniques in the area of signal integrity for high performance design.

**Description:** As designs are reaching Giga-Hertz clock rates, designers are increasingly forced to make trade-offs between the signal integrity and performance constraints for a design. In today's high performance designs, signal integrity arises from a number of complex issues and requires careful design and analysis of the power grid, circuit structures, and high speed interconnects.

The first part of this tutorial will give an overview of different signal integrity problems in a design and will demonstrate with industrial examples how they cause functional and performance failures. Also a brief overview of circuit extraction and interconnect modeling techniques will be covered.

Next, power grid signal integrity will be addressed, including resistive voltage drops, inductive voltage drops, and power grid resonance problems. Different power grid topologies and design methodologies will be discussed and illustrated with a number of industrial examples. The analysis approach and associated fast linear solution techniques will be presented.

The third part of this tutorial will focus on signal integrity of the circuits and interconnects. We will present different analysis approaches to evaluate cross coupling noise, and charge sharing noise and to determine if it causes functional failures. Also the effect of noise on the delay of the circuit will be addressed. We will present a number of examples of failures in industrial designs and will discuss methods for correcting noise problems.

The final part of the tutorial will discuss approaches for noise avoidance and emerging signal integrity issues, specifically self and mutual inductance, bipolar and floating body effects in SOI technologies, and signal integrity problems in ultra-low voltage designs with dual Vt technologies.