GENERAL INFORMATION AND HIGHLIGHTS

SUNDAY	NOVEMBER 7, 1999	
Early Registration (Bayshore Foyer)		5:00 PM - 8:00 PM
ACM/SIGDA Member Meeting (Donner Room)		5:30 PM

MONDAY	NOVEMBER 8, 1999	Page 18
Registration (Bayshore Foyer)		7:30 AM - 5:00 PM
Continental Breakfast (Sierra/Cascade Ballroom)		8:00 AM - 9:00 AM
Speakers' Breakfast (Monterey Room)		8:00 AM - 9:00 AM
Panel: CAD Roadmaps - Useful, Redundant or Even Obstructive? (Gateway Ballroom)		6:00 PM - 8:00 PM

TUESDAY	NOVEMBER 9, 1999	Page 32
Registration (Bayshore Foyer)		7:30 AM - 5:00 PM
Continental Breakfast (Sierra/Cascade Ballroom)		8:00 AM - 9:00 AM
Speakers' Breakfast (Monterey Room)		8:00 AM - 9:00 AM
Cocktail Reception (Sierra/Cascade Ballroom)		5:30 PM - 7:00 PM

WEDNESDAY	NOVEMBER 10, 1999	Page 40
Registration (Bayshore Foyer)		8:00 AM - 5:00 PM
Continental Breakfast (Sierra/Cascade Ballroom)		8:00 AM - 9:00 AM
Speakers' Breakfast (Monterey Room)		8:00 AM - 9:00 AM
ICCAD/ISSS Invited Papers (Pine/Fir Ballroom)		2:00 PM - 3:30 PM
ICCAD/ISSS Joint Session (Pine/Fir Ballroom)		4:00 PM - 5:30 PM
ICCAD/ISSS Panel: System-Level Design: Designers' Wish List vs. Reality (Gateway Ballroom)		6:00 PM - 7:30 PM

THURSDAY	NOVEMBER 11, 1999	Page 48
Continental Breakfast (Gateway Foyer)		8:00 AM - 9:00 AM
Tutorial Registration (Bayshore Foyer)		8:00 AM - 10:00 AM
Lunch (Gateway Foyer)		12:00 PM - 1:00 PM

ICCAD-99 AT A GLANCE

SUNDAY, NOVEMBER 7

Early Registration, 5:00 PM - 8:00 PM - (Bayshore Foyer)
ACM/SIGDAMember Meeting, 5:30 PM - (Donner Room)

MONDAY, NOVEMBER 8

Vendor Suites open by invitation
Continental Breakfast - 8:00 AM (Sierra/Cascade Ballroom)
Speakers' Breakfast - 8:00 AM - 8:30 AM (Monterey Room)

	Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom
9:00	1A Sequential and Datapath Optimization	1B Placement I	1C BDDs in Formal Verification	1D Analog and Mixed-Signal
10:30	**Coffee Break**			
11:00	2A Power Optimization	2B Placement II	2C Domino-and ATPG-Based Logic Synthesis	2D Electrical and Thermal Analysis
12:30	**Lunch (Sierra/Cascade Ballroom)**			
2:00	3A Automatic Test Pattern Generation	3B Routing	3C Logic-Level Performance Optimization	3D Practical Issues in Order Reduction
3:30	**Coffee Break**			
4:00	4A Embedded Tutorial: Formal Verification Meets Simulation (Donner/Siskiyou Ballroom)		4B Embedded Tutorial: Interconnect Parasitic Extraction in the Digital IC Design Methodology (Pine/Fir Ballroom)	
5:30	**Refreshments 5:30PM - 6:00PM**			
6:00	***PANEL: CAD ROADMAPS - USEFUL, REDUNDANT OR EVEN OBSTRUCTIVE?*** 6:00PM - 8:00PM (GATEWAY BALLROOM)			

ICCAD-99 AT A GLANCE

TUESDAY, NOVEMBER 9

Vendor Suites open by invitation
Continental Breakfast - 8:00 AM (Sierra/Cascade Ballroom)
Speakers' Breakfast - 8:00 AM - 8:30 AM (Monterey Room)

	Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom
9:00	5A Timing Optimization	5B Compilation Techniques for Embedded Systems	5C High Level Power Exploration	5D Analog and Mixed Signal Test
10:30	**Coffee Break**			
11:00	6A Globally Untimed Locally Timed Design	6B Task-Level Analysis and Synthesis	6C Floorplanning and Partitioning	6D Advances in Model Order Reduction
12:30	**Lunch (Sierra/Cascade Ballroom)**			
2:00	7A Core Test	7B Graph Techniques for Design Optimization	7C Interconnect	7D Techniques for Parasitic Extraction
3:30	**Coffee Break**			
4:00	8A Embedded Tutorial: SOI Technology and Tools (Donner/Siskiyou Ballroom)		8B Embedded Tutorial: System Level Design and Debug of High-Performance Embedded Media Systems (Pine/Fir Ballroom)	
5:30	**COCKTAIL RECEPTION** 5:30PM - 7:00PM (SIERRA /CASCADE BALLROOM)			

ICCAD-99 AT A GLANCE

WEDNESDAY, NOVEMBER 10

Vendor Suites open by invitation

Continental Breakfast - 8:00 AM (Sierra/Cascade Ballroom)

Speakers' Breakfast - 8:00 AM - 8:30 AM (Monterey Room)

	Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom
9:00	9A	9B	9C	9D
	Test Pattern Analysis	Memory and Interconnect Optimization in High Level Synthesis	System Verification	Fanout Optimization
10:30	**Coffee Break**			
11:00	10A	10B	10C	10D
	Timing Analysis	Concurrency in Embedded Systems	Semi-Formal Verification	Intellectual Property Protection
12:30	**Lunch (Sierra/Cascade Ballroom)**			
2:00	11A		11B	
	Embedded Tutorial: Path Toward Future CAD Environments for MEMS (Donner/Siskiyou Ballroom)		ICCAD/ISSS Invited Papers (Pine/Fir Ballroom)	
3:30	**Coffee Break**			
4:00	12A		12B	
	Embedded Tutorial: Advances in Transistsor Timing, Simulation, and Optimization (Donner/Siskiyou Ballroom)		Joint ICCAD/ISSS Session Embedded Tutorial: Embedded JAVA: Techniques and Applications (Pine/Fir Ballroom)	
5:30				

ICCAD/ISSS PANEL: SYSTEM LEVEL DESIGN: DESIGNERS' WISH LIST VS. REALITY

6:00 PM - 7:30 PM

(GATEWAY BALLROOM)

ICCAD-99 AT A GLANCE

Full-Day Tutorials

Continental Breakfast - 8:00AM - 9:00AM (Gateway Foyer)

Tutorial Registration - 8:00AM - 10:00AM (Bayshore Foyer)

Lunch - 12:00PM - 1:00PM (Gateway Foyer)

THURSDAY, NOVEMBER 11

9:00 AM **TUTORIAL 1** 5:00 PM

Mixed-Signal ASIC Design: CAD, Methodology, Case Studies

(CEDAR BALLROOM)

9:00 AM **TUTORIAL 2** 5:00 PM

Modern Physical Design: Algorithm, Technology and Methodology

(PINE BALLROOM)

9:00 AM **TUTORIAL 3** 5:00 PM

Low Voltage/Low Power Design Methodologies and CAD

(FIR BALLROOM)

9:00 AM **TUTORIAL 4** 5:00 PM

Signal Integrity in High Performance Design

(OAK BALLROOM)

MONDAY

SESSION 1A

Time: **9:00 AM to 10:30 AM** Room: **Cedar**

SEQUENTIAL AND DATAPATH OPTIMIZATION

Moderators: *Narendra V. Shenoy* - Synopsys, Inc., Mountain View, CA
Maurizio Damiani - C2 Design Automation, Santa Clara, CA

1A.1 MARSH: MIN-AREA RETIMING WITH SETUP AND HOLD CONSTRAINTS

V. Sundararajan *(vijay@ece.umn.edu), S. S. Sapatnekar, K. K. Parhi* - Univ. of Minnesota, Minneapolis, MN

1A.2 OPTIMISTA: STATE MINIMIZATION OF ASYNCHRONOUS FSMS FOR EXACTLY-OPTIMUM TWO-LEVEL OUTPUT LOGIC

R. M. Fuhrer (rmf@cs.columbia.edu), ***S. M. Nowick*** - Columbia Univ., New York, NY

1A.3 ARITHMETIC OPTIMIZATION FOR CARRY-SAVE ADDITIONS

K.-Y. Khoo, ***Z. Yu***, *A. N. Willson Jr. (willson@icsl.ucla.edu)* - Univ. of California, Los Angeles, CA

SESSION 1B

Time: **9:00 AM to 10:30 AM** Room: **Pine/Fir**

PLACEMENT I

Moderator: *Carl Sechen* - Univ. of Washington, Seattle, WA

1B.1 ATTRACTOR-REPELLER APPROACH FOR GLOBAL PLACEMENT

H. Etawil *(hussein@cheetah.vlsi.uwaterloo.ca), A. Vannelli* - Univ. of Waterloo, Waterloo, Canada
S. Areibi - Ryerson Polytechnic Univ., Toronto, Canada

1B.2 CELL REPLICATION AND REDUNDANCY ELIMINATION DURING PLACEMENT FOR CYCLE TIME OPTIMIZATION

I. Neumann *(ineumann@em.informatik.uni-frankfurt.de), D. Stoffel, W. Kunz* - J.W.G. Univ. Frankfurt, Germany
H. Hartje - Univ. Potsdam, Potsdam, Germany

1B.3 CONCURRENT LOGIC RESTRUCTURING AND PLACEMENT FOR TIMING CLOSURE

J. Lou *(jlou@sahand.usc.edu), W. Chen, M. Pedram* - Univ. of Southern California, Los Angeles, CA

All Speakers are denoted in bold
Email Addresses are for corresponding authors
S - denotes short paper

SESSION 1C

Time: **9:00 AM to 10:30 AM** Room: **Donner/Siskiyou**

BDDS IN FORMAL VERIFICATION

Moderators: *Andreas Kuehlmann* - IBM Corp., Yorktown Heights, NY
David L. Dill - Stanford Univ., Stanford, CA

1C.1 IMPLICIT ENUMERATION OF STRONGLY CONNECTED COMPONENTS

A. Xie *(aiguo@jungfrau.usc.edu)* - Cadence Design Systems, Inc., San Jose, CA
P.A. Beerel - Univ. of Southern California, Los Angeles, CA

1C.2 LEAST FIXPOINT APPROXIMATIONS FOR REACHABILITY ANALYSIS

I.-H. Moon *(mooni@vlsi.colorado.edu), F. Somenzi* - Univ. of Colorado, Boulder, CO
J. H. Kukula - Synopsys, Inc., Beaverton, OR
T. R. Shiple - Synopsys, Inc., Mountain View, CA

1C.3S LAZY GROUP SIFTING FOR EFFICIENT SYMBOLIC STATE TRAVERSAL OF FSMS

H. Higuchi *(higuchi@flab.fujitsu.co.jp)* - Fujitsu Labs. Ltd., Kawasaki, Japan
F. Somenzi - Univ. of Colorado, Boulder, CO

1C.4S EFFICIENT MANIPULATION ALGORITHMS FOR LINEARLY TRANSFORMED BDDS

W. Günther (*guenther@informatik.uni-freiburg.de*),
R. Drechsler - Univ. of Freiburg, Freiburg, Germany

SESSION 1D

Time: **9:00 AM to 10:30 AM** Room: **Oak**

ANALOG AND MIXED-SIGNAL

Moderators: *Balsha Robert Stanisic* - IBM Corp., Rochester, MN
Ramesh Harjani - Univ. of Minnesota, Minneapolis, MN

1D.1 NOISE ANALYSIS OF NON-AUTONOMOUS RADIO FREQUENCY CIRCUITS

A. Mehrotra *(mehrotra@eecs.berkeley.edu), A. L. Sangiovanni-Vincentelli* - Univ. of California, Berkeley, CA

1D.2S REDUCED ORDER ADAPTIVE HARMONIC BALANCE

B. J. Mulvaney (mulvaney@adttx.sps.mot.com),
K. K. Gullapalli - Motorola, Inc., Austin, TX
M. M. Gourary, ***S. G. Rusakov****, S. L. Ulyanov, M. M. Zharov* - Russian Academy of Sciences, Moscow, Russia

1D.3S DESIGN AND OPTIMIZATION OF LC OSCILLATORS

M. del Mar Hershenson *(marita@smirc.stanford.edu),*
S. Mohan, S. Boyd, T. Lee - Stanford Univ., Stanford, CA
A. Hajimiri - California Institute of Technology, Pasadena, CA

1D.4 MODELING AND SIMULATION OF THE INTERFERENCE DUE TO DIGITAL SWITCHING IN MIXED-SIGNAL ICS

A. Demir *(alpdemir@research.bell-labs.com),*
P. Feldmann - Bell Labs., Murray Hill, NJ

SESSION 2A

Time: **11:00 AM to 12:30 PM** Room: **Cedar**

POWER OPTIMIZATION

Moderators: *Renu Mehra* - Synopsys, Inc., Mountain View, CA
Luca Benini - Univ. of Bologna, Bologna, Italy

2A.1 PROVABLY GOOD ALGORITHM FOR LOW POWER CONSUMPTION WITH DUAL SUPPLY VOLTAGES

C. Chen, *M. Sarrafzadeh (majid@eecs.nwu.edu)* - Northwestern Univ., Evanston, IL

2A.2 A NOVEL DESIGN METHODOLOGYFOR HIGH PERFORMANCE AND LOW POWER DIGITALFILTERS

K. Muhammad *(khurram@ecn.purdue.edu)* - Texas Instruments, Dallas, TX,
K. Roy - Purdue Univ., West Lafayette, IN

2A.3 REDUCING POWER IN PIPELINED CIRCUITS - USING BIPARTITION-CODEC ARCHITECTURE

S.-J. Ruan, *R.-J. Shang*, ***F. Lai*** *(flai@cc.ee.ntu.edu.tw)* - National Taiwan Univ., Taiwan, ROC

SESSION 2B

Time: **11:00 AM to 12:30 PM** Room: **Pine/Fir**

PLACEMENT II

Moderators: *Majid Sarrafzadeh* - Northwestern Univ., Evanston, IL
Gary Yeap - Monterey Design Systems Inc., Sunnyvale, CA

2B.1 AKORD: TRANSISTOR LEVEL AND MIXED TRANSISTOR/GATE LEVEL PLACEMENT TOOL FOR DIGITAL DATA PATHS

T. Serdar *(tatjana@twolf13.ee.washington.edu)*,
C. Sechen - Univ. of Washington, Seattle, WA

2B.2 ANALYTICAL APPROACH TO CUSTOM DATAPATH DESIGN

S. Askar, *M. Ciesielski (ciesiel@illiac.ecs.umass.edu)* - Univ. of Massachusetts, Amherst, MA

2B.3 AN INTEGRATED ALGORITHM FOR COMBINED PLACEMENT AND LIBRARYLESS TECHNOLOGY MAPPING

Y. Jiang - Cadence Design Systems, Inc., San Jose, CA
S. S. Sapatnekar (sachin@ece.umn.edu) - Univ. of Minnesota, Minneapolis, MN

All Speakers are denoted in bold
Email Addresses are for corresponding authors

S - denotes short paper

SESSION 2C

Time: **11:00 AM to 12:30 PM** Room: **Donner/Siskiyou**

DOMINO-AND ATPG-BASED LOGIC SYNTHESIS

Moderators: *Rajeev Murgai* - Fujitsu Labs. of America, Inc., Sunnyvale, CA
Massoud Pedram - Univ. of Southern California, Los Angeles, CA

2C.1 TIMING-DRIVEN PARTITIONING FOR TWO-PHASE DOMINO AND MIXED STATIC/DOMINO IMPLEMENTATIONS

M. Zhao, *S. S. Sapatnekar (sachin@ece.umn.edu)* - Unvi. of Minnesota, Minneapolis, MN

2C.2 IMPLICATION GRAPH BASED DOMINO LOGIC SYNTHESIS

K.-W. Kim *(kkim7@uiuc.edu)*, *S.-M. Kang* - Univ. of Illinois, Urbana, IL
C. L. Liu - National Tsing Hua Univ., Taiwan, ROC

2C.3 SYNTHESIS OF MULTIPLE INPUT WIRES REPLACEMENT FOR WIRING CONSIDERATION

S.-C. Chang *(scchang@cs.ccu.edu.tw)*, *J.-C. Chuang*, *Z.-Z. Wu* - National Chung-Cheng Univ., Taiwan, ROC

SESSION 2D

Time: **11:00 AM to 12:30 PM** Room: **Oak**

ELECTRICAL AND THERMAL ANALYSIS

Moderators: *Joel R. Phillips* - Cadence Design Systems, Inc., San Jose, CA
Peter Feldmann - Bell Labs., Murray Hill, NJ

2D.1 TRANSIENT SENSITIVITY COMPUTATION FOR TRANSISTOR LEVEL ANALYSIS AND TUNING

T. V. Nguyen (tuyenn@austin.ibm.com), *P. O'Brien* - IBM Austin Research Lab., Austin, TX
D. Winston - IBM Electronic Design Automation, Hopewell Junction, NY

2D.2S AN EFFICIENT METHOD FOR HOT-SPOT IDENTIFICATION IN ULSI CIRCUITS

Y.-K. Cheng (yikan@ibmoto.com) - Motorola Inc., Austin, TX
S.-M. (Steve) Kang - Univ. of Illinois, Urbana, IL

2D.3S A SCALABLE SUBSTRATE NOISE COUPLING MODEL FOR MIXED-SIGNAL ICS

A. Samavedam *(asamaved@eecs.wsu.edu)*, *K. Mayaram*, *T. S. Fiez* - Washington State Univ., Pullman, WA

2D.4 TRUE CROSSTALK NOISE ANALYSIS

P. Chen *(pinhong@eecs.berkeley.edu)*, *K. Keutzer* - Univ. of California, Berkeley, CA

SESSION 3A

Time: **2:00 PM to 3:30 PM** Room: **Cedar**

AUTOMATIC TEST PATTERN GENERATION

Moderators: *Janak H. Patel* - Univ. of Illinois, Urbana, IL
Vamsi Boppana - Fujitsu Labs. of America, Sunnyvale, CA

3A.1 SAT BASED ATPG USING FAST JUSTIFICATION AND PROPAGATION IN THE IMPLICATION GRAPH

P. Tafertshofer *(tafertshofer@eda.ei.tum.de)*, *A. Ganz* - Technical Univ. of Munich, Munich, Germany

3A.2 TECHNIQUES FOR IMPROVING THE EFFICIENCY OF SEQUENTIAL CIRCUIT TEST GENERATION

X. Lin *(xijiang_lin@mentorg.com)* - Mentor Graphics Corp., Wilsonville, OR
I. Pomeranz, *S. M. Reddy* - Univ. of Iowa, Iowa City, IA

3A.3 CONCURRENT D-ALGORITHM ON RECONFIGURABLE HARDWARE

F. Kocan, *D. G. Saab (dgs3@po.cwru.edu)* - Case Western Reserve Univ., Cleveland, OH

SESSION 3B

Time: **2:00 PM to 3:30 PM** Room: **Pine/Fir**

ROUTING

Moderators: *Patrick Groeneveld* - Magma Design Automation, Inc., Cupertino, CA
Louis Scheffer - Cadence Design Systems, Inc., San Jose, CA

3B.1 A NEW HEURISTIC FOR RECTILINEAR STEINER TREES

I. Mandoiu *(mandoiu@cc.gatech.edu)*, *V. Vazirani* - Georgia Institute of Technology, Atlanta, GA
J. Ganley - Simplex Solutions, Inc., Sunnyvale, CA

3B.2 AN IMPLICIT CONNECTION GRAPH MAZE ROUTING ALGORITHM FOR ECO ROUTING

J. Cong, ***J. Fang*** (*jfang@cs.ucla.edu)*, *K. Y. Khoo* - Univ. of California, Los Angeles, CA

3B.3S ON THE ASSOCIATIVE-SKEW CLOCK ROUTING PROBLEM

A. B. Kahng, *Y. Chen,* G. Qu - Univ. of California, Los Angeles, CA
A. Zelikovsky (alexz@cs.gsu.edu) - Georgia State Univ., Atlanta, GA

3B.4S EFFICIENT INCREMENTAL REROUTING FOR FAULT RECONFIGURATION IN FIELD PROGRAMMABLE GATE ARRAYS

S. Dutt *(dutt@eecs.uic.edu)*, *V. Shanmugavel* - Univ. of Illinois, Chicago, IL
S. Trimberger - Xilinx, Inc., San Jose, CA

SESSION 3C

Time: **2:00 PM to 3:30 PM** Room: **Donner/Siskiyou**

LOGIC-LEVEL PERFORMANCE OPTIMIZATION

Moderators: *Masahiro Fujita* - Fujitsu Labs. of America, Inc., Sunnyvale, CA
Hamid Savoj - Magma Design Automation, Inc., Cupertino, CA

3C.1 OPTIMAL P/N WIDTH RATIO SELECTION FOR STANDARD CELL LIBRARIES

D. Kung, ***R. Puri*** *(puri@watson.ibm.com)* - IBM Corp., Yorktown Heights, NY

3C.2 PERFORMANCE OPTIMIZATION UNDER RISE AND FALL PARAMETERS

R. Murgai *(murgai@fla.fujitsu.com)* - Fujitsu Labs. of America, Inc., Sunnyvale, CA

3C.3S PERFORMANCE OPTIMIZATION USING SEPERATOR SETS

Y. Tamiya *(tamy@flab.fujitsu.co.jp)* - Fujitsu Labs., Ltd., Kawasaki, Japan

3C.4S FACTORING LOGIC FUNCTIONS USING GRAPH PARTITIONING

A. Mintz *(mintz@cs.biu.ac.il)* - Bar Ilan Univ., Ramat Gan, Israel

SESSION 3D

Time: **2:00 PM to 3:30 PM** Room: **Oak**

PRACTICAL ISSUES IN ORDER REDUCTION

Moderators: *Luis Miguel Silveira* - INESC, Lisboa, Portugal
Tuyen V. Nguyen - IBM Austin Research Lab., Austin, TX

3D.1 TICER: REALIZABLE REDUCTION OF EXTRACTED RC CIRCUITS

B. N. Sheehan *(bernie_sheehan@mentorg.com)* - Mentor Graphics Corp., Wilsonville, OR

3D.2S REALIZABLE REDUCTION FOR RC INTERCONNECT CIRCUITS

A. Devgan *(devgan@austin.ibm.com)*, *P. O'Brien* - IBM Corp., Austin, TX

3D.3S RLC INTERCONNECT DELAY ESTIMATION VIA MOMENTS OF AMPLITUDE AND PHASE RESPONSE

X. Yang (*xdyang@cs.ucsd.edu)*, *W .H. Ku*, *C.-K. Cheng* - Univ. of California at San Diego, La Jolla, CA

3D.4 PRACTICAL CONSIDERATIONS FOR PASSIVE REDUCTION OF RLC CIRCUITS

A. Odabasioglu *(altan@montereydesign.com)*, *M. Celik* - Monterey Design Systems, Sunnyvale, CA
L. T. Pileggi - Carnegie Mellon Univ., Pittsburgh, PA

SESSION 4A

Time: **4:00 PM to 5:30 PM** Room: **Donner/Siskiyou**

EMBEDDED TUTORIAL: FORMAL VERIFICATION MEETS SIMULATION

Moderator: *Ellen Sentovich* - Cadence Berkeley Labs., Berkeley, CA

This embedded tutorial explores some of the options for verification in the territory between current methods based simulation and emulation, and formal verification. Topics covered will include: coverage metrics and their effectiveness at uncovering bugs, symbolic simulation for partial formal verification, and directed search of a design.

PRESENTERS:

David L. Dill - Stanford Univ., Stanford, CA
Serdar Tasiran - Univ. of California, Berkeley, CA

SESSION 4B

Time: **4:00 PM to 5:30 PM** Room: **Pine/Fir**

EMBEDDED TUTORIAL: INTERCONNECT PARASITIC EXTRACTION IN THE DIGITAL IC DESIGN METHODOLOGY

Moderator: *Lawrence T. Pileggi* - Carnegie Mellon Univ., Pittsburg, PA

With increasing circuit speeds and chip densities, consideration of interconnect parasitics must be both more accurate and sophisticated, as well as occur increasingly early in the IC design process. In the design planning stage, this means more accurate estimation techniques to guide design decisions and to enable more "correct-by-construction" synthesis. In the post-layout verification stage, this requires the solution of a complex parasitic extraction and analysis problem on an exploding amount of data. In this tutorial, we discuss post-layout parasitic extraction as well as approaches to parasitic-aware synthesis.

We begin by discussing the electrical issues that require detailed understanding of parasitics. These include accurate timing, noise, electromigration, and power-supply integrity analysis. We will consider the relative importance of resistance, capacitance, and inductance in these analyses, and also the influence of new technology (e.g. Cu) and scaling. We briefly consider modern approaches to capacitance extraction that include scan-band algorithms combined with analytical or table-look-up models and then consider extending these techniques for inductance. We consider the real accuracy requirements of extraction and the importance of manufacturing tolerances.

We briefly enumerate the current approaches to model-order reduction, which has become the essential link between the large number of extracted RLC parasitic circuit elements and practical electrical analysis.

Any RLC extraction method must solve Maxwell's equations at some level. While previously, the need for solution could be limited to the calibration of table-look-up extractors, more recently, increasing frequencies have moved board-level issues on-chip and the lines between circuit theory and field theory have become increasingly blurred. We will discuss efficient approaches to the necessary 3D electromagnetic analysis, from quasistatic to full-wave. Because the extraction can no longer practically be separated from model reduction, we will discuss approaches to generate low order models DIRECTLY from Maxwell's equations.

If a large number of electrical problems are not discovered until after layout, significant redesign and rework will be necessary. As a result, electrical correctness must be engineered into the entire IC design process. In the final talk of this tutorial, we consider how correctness can be built into the interconnect design environment by controlling lengths (through placement), coupling (through congestion control in placement) and circuit immunity to noise (through driver sizing and buffer insertion). Detailed routers must also understand length, width and adjacency criticality. These needs demand accurate interconnect estimates to drive placement, synthesis, and routings, which we also discuss.

PRESENTERS:

Mattan Kamon - Microcosm Technologies, Inc., Cambridge, MA
Kenneth L. Shepard - Columbia Univ., New York, NY
Steven P. McCormick - Sapphire Design Automation, Santa Clara, CA

Time: **6:00 PM to 8:00 PM** Room: **Gateway Ballroom**

PANEL: CAD ROADMAPS - USEFUL, REDUNDANT OR EVEN OBSTRUCTIVE?

Moderator: *Rolf Ernst* - Technical Univ. of Braunschweig, Braunschweig, Germany

There will be a new edition of the SIA roadmap this year. The SIA roadmap has been used by the semiconductor industry to develop new products and technologies in close synchronization. The SIA roadmap also contains a CAD section which defines the tools necessary to make the predicted technological progress happen.

In general, roadmaps are developed to support management decisions and to control longer term technological innovation, and - in this context - define relevant fields for academic research. Despite a much smaller size, the EDA industry experiences similar delay times from academic research to widely accepted products. Complex interdependencies between CAD tools, IPlibraries, standardization processes and company design methodologies make predictions difficult. Embedded system design added additional hooks to the world of software development. So, reliable CAD roadmaps could be a valuable decision support for the EDA, semiconductor and systems industries.

On the other hand, roadmap prophecies, if taken serious, tend to be self-fulfilling due to their influence on technological investments and, eventually, on research funds. So, roadmaps could potentially stifle innovation especially in a highly dynamic area such as system design.

The distinguished panel will discuss the usefulness and the impact of CAD roadmaps. It includes authors of the SIA roadmap, of Asian and European CAD roadmaps, as well as highly influential representatives from academia and from the EDA industry.

PANEL MEMBERS

Ivo Bolsens - IMEC, Leuven, Belgium
Raul Camposano - Synopsys, Inc., Mountain View, CA
Tamotsu Hiwatashi - Toshiba Corp., Kawasaki, Japan
William Joyner - SRC, Research Triangle Park, NC
Edward A. Lee - Univ. of California, Berkeley, CA
Richard Newton - Univ. of California, Berkeley, CA
Gabriele Saucier - IMAG, Grenoble, France

TUESDAY

SESSION 5A

Time: **9:00 AM to 10:30 AM** Room: **Cedar**

TIMING OPTIMIZATION

Moderator: *Alexander T. Ishii* - NEC USA, C&C Research Labs., Princeton, NJ

5A.1 CYCLE TIME AND SLACK OPTIMIZATION FOR VLSI-CHIPS

C. Albrecht, B. Korte, *J. Schietke*, ***J. Vygen*** (vygen@or.uni-bonn.de) - Univ. of Bonn, Bonn, Germany

5A.2 CLOCK SKEW SCHEDULING FOR IMPROVED RELIABILITY VIA QUADRATIC PROGRAMMING

I. S. Kourtev - Univ. of Pittsburgh, Pittsburgh, PA
E. G. Friedman (friedman@ece.rochester.edu) - Univ. of Rochester, Rochester, NY

5A.3 FORMULATION OF STATIC CIRCUIT OPTIMIZATION WITH REDUCED SIZE, DEGENERACY AND REDUNDANCY BY TIMING GRAPH MANIPULATION

C. Visweswariah *(chandu@watson.ibm.com)*, *A. R. Conn* - IBM Corp., Yorktown Heights, NY

SESSION 5B

Time: **9:00 AM to 10:30 AM** Room: **Pine/Fir**

COMPILATION TECHNIQUES FOR EMBEDDED SYSTEMS

Moderators: *Abhijit Ghosh* - Synopsys, Inc., Mountain View, CA
Donatella Sciuto - Politecnico di Milano, Milano, Italy

5B.1 FUNCTION INLINING UNDER CODE SIZE CONSTRAINTS FOR EMBEDDED PROCESSORS

R. Leupers (leupers@ls12.cs.uni-dortmund.de), ***P. Marwedel*** - Univ. of Dortmund, Dortmund, Germany

5B.2 FUNCTIONAL UNIT SPECIALIZATION THROUGH CODE ANALYSIS

D. Benyamin *(benyamin@ucla.edu)*, *W. H. Mangione-Smith* - Univ. of California, Los Angeles, CA

5B.3 LOWER BOUND ON LATENCY FOR VLIW ASIP DATAPATHS

M. Jacome *(jacome@ece.utexas.edu)*, G. de Veciana - Univ. of Texas, Austin, TX

All Speakers are denoted in bold
Email Addresses are for corresponding authors
S - denotes short paper

SESSION 5C

Time: **9:00 AM to 10:30 AM** Room: **Donner/Siskiyou**

HIGH LEVEL POWER EXPLORATION

Moderators: *Farid N. Najm* - Univ. of Toronto, Toronto, Canada
Kaushik Roy - Purdue Univ., West Lafayette, IN

5C.1 INTERFACE AND CACHE POWER EXPLORATION FOR CORE-BASED EMBEDDED SYSTEM DESIGN

T. Givargis *(givargis@cs.ucr.edu)*, *F. Vahid* - Univ. of California, Riverside, CA
J. Henkel - NEC USA, C&C Research Labs., Princeton, NJ

5C.2 DYNAMIC POWER MANAGEMENT USING ADAPTIVE LEARNING TREE

E.-Y. Chung *(eychung@stanford.edu)*, *G. De Micheli* - Stanford Univ., Stanford, CA
L. Benini - Univ. of Bologna, Bologna, Italy

5C.3S ANALYTICAL MACRO-MODELING FOR HIGH-LEVEL POWER ESTIMATION

G. Bernacchia (bernac@eecs.umich.edu), ***M. C. Papaefthymiou*** - Univ. of Michigan, Ann Arbor, MI

5C.4S PARAMETERIZED RTL POWER MODELS FOR COMBINATIONAL SOFT MACROS

A. Bogliolo - Univ. of Bologna, Bologna, Italy
R. Corgnati, ***E. Macii***, M. Poncino (poncino@athena.polito.it) - Politecnico di Torino, Torino, Italy

SESSION 5D

Time: **9:00 AM to 10:30 AM** Room: **Oak**

ANALOG AND MIXED SIGNAL TEST

Moderators: *Kwang-Ting (Tim) Cheng* - Univ. of California, Santa Barbara, CA
Shawn Blanton - Carnegie Mellon Univ., Pittsburgh, PA

5D.1 VALIDATION AND TEST GENERATION FOR OSCILLATORY NOISE IN VLSI INTERCONNECTS

A. Sinha, *S. K. Gupta (sandeep@poisson.usc.edu)*, *M. A. Breuer* - Univ. of Southern California, Los Angeles, CA

5D.2 FAULT MODELING AND SIMULATION FOR CROSSTALK IN SYSTEM-ON-CHIP BUS INTERCONNECTS

M. Cuviello (mcuviell@ece.ucsd.edu), ***S. Dey***, *X. Bai*, *Y. Zhao* - Univ. of California at San Diego, La Jolla, CA

5D.3 ROBUST OPTIMIZATION BASED BACKTRACE METHOD FOR ANALOG CIRCUITS

A. V. Gomes *(vgomes@ee.gatech.edu)*, *A. Chatterjee* - Georgia Institute of Technology, Atlanta, GA

SESSION 6A

Time: **11:00 AM to 12:30 PM** Room: **Cedar**

GLOBALLY UNTIMED LOCALLY TIMED DESIGN

Moderators: *Kenneth Y. Yun* - Univ. of California at San Diego, La Jolla, CA
Steven M. Nowick - Columbia Univ., New York, NY

6A.1 A METHODOLOGY FOR CORRECT-BY-CONSTRUCTION LATENCY INSENSITIVE DESIGN

L. P. Carloni (*lcarloni@ic.eecs.berkeley.edu)*, *A. L. Sangiovanni-Vincentelli* - Univ. of California, Berkeley, CA
K. L. McMillan, *A. Saldanha* - Cadence Design Systems, Inc., Berkeley, CA

6A.2 WHAT IS THE COST OF DELAY INSENSITIVITY

A. Kondratyev *(kondraty@u-aizu.ac.jp)*, *H. Saito* - Univ. of Aizu, Fukushima, Japan
J. Cortadella - Univ. Politecnica de Catalunya, Barcelona, Spain
L. Lavagno - Univ. di Udine, Udine, Italy
A. Yakovlev - Univ. of Newcastle Upon Tyne, Newcastle Upon Tyne, UK

6A.3S SYNTHESIS OF ASYNCHRONOUS CONTROL CIRCUITS WITH AUTOMATICALLY GENERATED RELATIVE TIMING ASSUMPTIONS

J. Cortadella (jordic@lsi.upc.es) - Univ. Politecnica de Catalunya, Barcelona, Spain
M. Kishinevsky, *S. Burns*, *K. Stevens* - Intel Corp., Hillsboro, OR

6A.4S DIRECT SYNTHESIS OF TIMED ASYNCHRONOUS CIRCUITS

S. Jung *(stjung@ming.elen.utah.edu)*, *C. J. Myers* - Univ. of Utah, Salt Lake City, UT

SESSION 6B

Time: **11:00 AM to 12:30 PM** Room: **Pine/Fir**

TASK-LEVEL ANALYSIS AND SYNTHESIS

Moderators: *Francky Catthoor* - IMEC, Leuven, Belgium
Stan Liao - Synopsys, Inc., Mountain View, CA

6B.1 CO-SYNTHESIS OF HETEROGENEOUS MULTIPROCESSOR SYSTEMS USING ARBITRATED COMMUNICATION

D. Rhodes *(dlr@ee.princeton.edu)*, *W. Wolf* - Princeton Univ., Princeton, NJ

6B.2 POWER MINIMIZATION USING SYSTEM-LEVEL PARTITIONING OF APPLICATIONS WITH QUALITY OF SERVICE REQUIREMENTS

G. Qu *(gangqu@cs.ucla.edu)*, *M. Potkonjak* - Univ. of California, Los Angeles, CA

6B.3 WORST-CASE ANALYSIS OF DISCRETE SYSTEMS

F. Balarin *(felice@cadence.com)* - Cadence Berkeley Labs., Berkeley, CA

SESSION 6C

Time: **11:00 AM to 12:30 PM** Room: **Donner/Siskiyou**

FLOORPLANNING AND PARTITIONING

Moderators: *Naveed Sherwani* - Intel Corp., Hillsboro, OR
D. F. Wong - Univ. of Texas, Austin, TX

6C.1 INTEGRATED FLOORPLANNING AND INTERCONNECT PLANNING

H.-M.Chen, *H. Zhou*, *F. Y. Young*, *D. F. Wong* (wong@cs.utexas.edu) - Univ. of Texas, Austin, TX
H. Yang, *N. Sherwani* - Intel Corp., Hillsboro, OR

6C.2 BUFFER BLOCK PLANNING FOR INTERCONNECT-DRIVEN FLOORPLANNING

J. Cong (cong@cs.ucla.edu), *T. Kong*, ***D. Z. Pan*** - Univ. of California, Los Angeles, CA

6C.3 A CLUSTERING - AND PROBABILITY-BASED APPROACH FOR TIME-MULTIPLEXED FPGAS PARTITIONING

M. C.-T.Chao, *G. M. Wu*, *I. H. R. Jiang*, *Y.-W. Chang* (ywchang@cis.nctu.edu.tw) - National Chiao Tung Univ., Taiwan, ROC

SESSION 6D

Time: **11:00 AM to 12:30 PM** Room: **Oak**

ADVANCES IN MODEL ORDER REDUCTION

Moderators: *Ibrahim M. Elfadel* - IBM Corp., Yorktown Heights, NY
Alper Demir - Bell Labs., Murray Hill, NJ

6D.1 THE CHEBYSHEV EXPANSION BASED PASSIVE MODEL FOR DISTRIBUTED INTERCONNECT NETWORKS

J. M. L. Wang *(wml@eecs.berkeley.edu)* - Univ. of California, Berkeley, CA

6D.2 MODEL REDUCTION FOR DC SOLUTION OF LARGE NONLINEAR CIRCUITS

E. Gad, *M. Nakhla (msn@doe.carleton.ca)* - Carleton Univ., Ottawa, Canada

6D.3 EFFICIENT MODEL REDUCTION OF INTERCONNECT VIAAPPROXIMATE SYSTEM GRAMMIANS

J. R. Li *(jingli@math.mit.edu)*, *J. K. White* - Massachusetts Institute of Technology, Cambridge, MA

All Speakers are denoted in bold
Email Addresses are for corresponding authors
S - denotes short paper

SESSION 7A

Time: **2:00 PM to 3:30 PM** Room: **Cedar**

CORE TEST

Moderators: *Srinivas Patil* - Mentor Graphics Corp., Austin, TX
Nur A. Touba - Univ. of Texas, Austin, TX

7A.1 A FRAMEWORK FOR TESTING CORE-BASED SYSTEMS-ON-A-CHIP

S. Ravi *(sravi@ee.princeton.edu)*, *N. Jha* - Princeton Univ., Princeton, NJ
G. Lakshminarayana - NEC USA, Princeton, NJ

7A.2 TEST SCHEDULING FOR CORE-BASED SYSTEMS

K. Chakrabarty *(krish@ee.duke.edu)* - Duke Univ., Durham, NC

7A.3 PARTIAL BIST INSERTION TO ELIMINATE DATA CORRELATION

Q. Zhang, *I. G. Harris (harris@ecs.umass.edu)* - Univ. of Massachusetts, Amherst, MA

SESSION 7B

Time: **2:00 PM to 3:30 PM** Room: **Pine/Fir**

GRAPH TECHNIQUES FOR DESIGN OPTIMIZATION

Moderators: *Sujit Dey* - Univ. of California, San Diego, La Jolla, CA
Don MacMillen - Synopsys, Inc., Mountain View, CA

7B.1 A GRAPH THEORETIC OPTIMAL ALGORITHM FOR SCHEDULE COMPRESSION IN TIME-MULTIPLEXED FPGA PARTITIONING

H. Liu *(hqliu@cs.utexas.edu)*, *D. F. Wong* - Univ. of Texas, Austin, TX

7B.2 THROUGHPUT OPTIMIZATION OF GENERAL NON-LINEAR COMPUTATIONS

I. Hong - Synopsys, Inc., Mountain View, CA
M. Potkonjak *(miodrag@cs.ucla.edu)* - Univ. of California, Los Angeles, CA
L. M. Guerra - Rockwell Semiconductor, Newport Beach, CA

7B.3S OPTIMAL ALLOCATION OF CARRY-SAVE-ADDERS IN ARITHMETIC OPTIMIZATION

J. Um *(jhum@jupiter.kaist.ac.kr)*, *T. Kim* - Korea Advanced Institute of Science and Technology, Taejon, Korea
C. L. Liu - National Tsing Hua Univ., Taiwan, ROC

7B.4S REGULARITY EXTRACTION VIA CLAN-BASED STRUCTURAL CIRCUIT DECOMPOSITION

S. Hassoun *(soha@eecs.tufts.edu)*, *C. McCreary* - Tufts Univ., Medford, MA

SESSION 7C

Time: **2:00 PM to 3:30 PM** Room: **Donner/Siskiyou**

INTERCONNECT

Moderators: *Jochen A.G. Jess* - Eindhoven Univ. of Tech., Eindhoven, The Netherlands
Rajesh K. Gupta - Univ. of California, Irvine, CA

7C.1 REPEATER INSERTION IN TREE STRUCTURED INDUCTIVE INTERCONNECT

Y. Ismail *(ismail@ece.rochester.edu)*, *E. G. Friedman* - Univ. of Rochester, Rochester, NY
J. L. Neves - IBM Microelectronics, East Fishkill, NY

7C.2 INTERCONNECT SCALING IMPLICATIONS FOR CAD

R. Ho, *K. Mai (demon@vlsi.stanford.edu)*, *H. Kapadia*, *M. Horowitz* - Stanford Univ., Stanford, CA

7C.3 IS WIRE TAPERING WORTHWHILE?

C. J. Alpert *(alpert@austin.ibm.com)*, *A. Devgan* - IBM Corp., Austin, TX
S. T. Quay - IBM Microelectronics, Austin, TX

SESSION 7D

Time: **2:00 PM to 3:30 PM** Room: **Oak**

TECHNIQUES FOR PARASITIC EXTRACTION

Moderators: *J. Eric Bracken* - Ansoft Corp., Pittsburgh, PA
Keith Nabors - Cadence Design Systems, Inc., San Jose, CA

7D.1 ELECTROMAGNETIC PARASITIC EXTRACTION VIA A MULTIPOLE METHOD WITH HIERARCHICAL REFINEMENT

M. W. Beattie *(beattie@ece.cmu.edu)*, *L. T. Pileggi* - Carnegie Mellon Univ., Pittsburgh, PA

7D.2 VIRTUAL SCREENING: A STEP TOWARDS A SPARSE PARTIAL INDUCTANCE MATRIX

A. J. Dammers, ***N. P. van der Meijs*** *(nick@cas.et.tudelft.nl)* - Delft Univ. of Technology, Delft, The Netherlands

7D.3 A WIDE FREQUENCY RANGE SURFACE INTEGRAL FORMULATION FOR 3-D RLC EXTRACTION

J. Wang *(jfwang@rle-vlsi.mit.edu)*, *J. K. White* - Massachusetts Institute of Technology, Cambridge, MA
J. Tausch - Southern Methodist Univ., Dallas, TX

All Speakers are denoted in bold
Email Addresses are for corresponding authors
S - denotes short paper

SESSION 8A

Time: **4:00 PM to 5:30 PM** Room: **Donner/Siskiyou**

EMBEDDED TUTORIAL: SOI TECHNOLOGY AND TOOLS

Moderator: *Lawrence T. Pileggi* - Carnegie Mellon Univ., Pittsburgh, PA

SOI represents a technology shift comparable in impact to the shift from NMOS to CMOS. It has impacts on many aspects of modeling, simulation and analysis, and presents some unique challenges due to the presence of a number of electrical phenomena unique to SOI.

In this tutorial, we will review SOI technology, touching specifically on devices and models, as well as the impact of the floating body and parasitic bipolar effects. We show examples of the impact of these electrical phenomena on circuit behavior and balance that against existing sources of variation such as power supply variations, signal-to-signal coupling and processing fluctuations. We will then show the impact of these phenomena on relevant areas of ECAD such as circuit simulation, timing (or fast circuit) simulation, static timing analysis, power and thermal estimation, synthesis/technology mapping and physical design.

PRESENTERS:

Sani Nassif - IBM Austin Research Lab., Austin, TX
Tuyen Nguyen - IBM Austin Research Lab., Austin, TX

SESSION 8B

Time: **4:00 PM to 5:30 PM** Room: **Pine/Fir**

EMBEDDED TUTORIAL: SYSTEM LEVEL DESIGN AND DEBUG OF HIGH-PERFORMANCE EMBEDDED MEDIA SYSTEMS

Moderator: *Rolf Ernst* - Tech. Univ. of Braunschweig, Braunschweig, Germany

This tutorial on System Level Design practices in Philips consists of three parts. In the first part we discuss application domain characteristics and architectures for video processing. High performance video processing applications impose severe demands on architectures. The architectures need to provide both high bandwidth for communication and high processing power for computation. Such architectures often consist of a combination of programmable cores and more dedicated coprocessors. This is illustrated with the TriMedia based VLIW cores combined with dedicated coprocessors, e.g. an HD resolution MPEG-2 decoder and a dedicated video output processing unit.

Several architectures that are developed within Philips will be illustrated. These include the programmable TriMedia VLIW media processor, a dataflow style stream processing architecture, and more dedicated solutions for video processing. Furthermore the future trend of building platforms out of these components will be illustrated.

In the second part we discuss the design technology that is employed to perform architecture modeling and evaluation and design space exploration. During the initial stages of architecture design several decisions with a large impact are taken. In Philips, practice is developed to model architectures at a high level of abstraction. With such models architectural options can be explored quantitatively. Such explorations are driven by a suite of characteristic benchmark applications. Several levels of architecture modeling will be illustrated. Methods and tools used for exploration of both a multiprocessor system including a dedicated MPEG-2 decoder and a future VLIW core will be presented.

In the third part we discuss a methodology for System-On-a-Chip debug. For today's multi-million transistor designs, existing design verification techniques cannot guarantee that first silicon is designed error free. Therefore, techniques are necessary to quickly debug first-silicon. In this presentation, we present a methodology for debugging multiple clock domain systems-on-a-chip. The methodology supports the insertion of special debug components in the design (Design-for-Debug). After silicon becomes available debugger tool software is used to interact with these components to enable silicon debugging from a workstation. The tool software provided features such as the ones commonly found in simulation environments e.g. breakpoints and virtual probes. The application of these techniques to a dataflow style video processor will be illustrated.

PRESENTERS:

Kees A. Vissers - Philips Research Labs., Eindhoven, The Netherlands
Pieter van der Wolf - Philips Research Labs., Eindhoven, The Netherlands
Gert-Jan van Rootselaar - Philips Research Labs., Eindhoven, The Netherlands

SESSION 9A

Time: **9:00 AM to 10:30 AM** Room: **Cedar**

TEST PATTERN ANALYSIS

Moderators: *Robert Aitken* - Hewlett-Packard Co., Palo Alto, CA
Sreejit Chakravarty - Intel Corp., Santa Clara, CA

9A.1 AN APPROACH FOR IMPROVING THE LEVELS OF COMPACTION ACHIEVED BY VECTOR OMISSION

I. Pomeranz *(irith@eng.uiowa.edu)*, *S. M. Reddy* - Univ. of Iowa, Iowa City, IA

9A.2 DEEP SUBMICRON DEFECT DETECTION WITH THE ENERGY CONSUMPTION RATIO

B. Vinnakota *(bapi@ece.umn.edu)* - Univ. of Minnesota, Minneapolis, MN

9A.3 EFFICIENT DIAGNOSIS OF PATH DELAY FAULTS IN DIGITAL LOGIC CIRCUITS

P. Pant *(pant@ee.gatech.edu)*, *A. Chatterjee* - Georgia Institute of Technology, Atlanta, GA

SESSION 9B

Time: **9:00 AM to 10:30 AM** Room: **Pine/Fir**

MEMORY AND INTERCONNECT OPTIMIZATION IN HIGH LEVEL SYNTHESIS

Moderator: *Kazutoshi Wakabayashi* - NEC Corp., Kawasaki, Japan

9B.1 MEMORY BANK CUSTOMIZATION AND ASSIGNMENT IN BEHAVIORAL SYNTHESIS

P. R. Panda *(panda@synopsys.com)* - Synopsys, Inc., Mountain View, CA

9B.2 MEMORY BINDING FOR PERFORMANCE OPTIMIZATION OF CONTROL-FLOW INTENSIVE BEHAVIORS

K. S. Khouri *(kskhouri@ee.princeton.edu)*, *N. Jha* - Princeton Univ., Princeton, NJ
G. Lakshminarayana - NEC USA, Princeton, NJ

9B.3 IMPROVED INTERCONNECT SHARING BY IDENTITY OPERATION INSERTION

D. Herrmann *(d.herrmann@tu-bs.de)*, *R. Ernst* - Technical Univ. of Braunschweig, Braunschweig, Germany

All Speakers are denoted in bold
Email Addresses are for corresponding authors
S - denotes short paper

SESSION 9C

Time: **9:00 AM to 10:30 AM** Room: **Donner/Siskiyou**

SYSTEM VERIFICATION

Moderators: *Mandayam Srivas* - SRI International, Menlo Park, CA
Pei-Hsin Ho - Synopsys Inc., Beaverton, OR

9C.1 FORMAL SPECIFICATION AND VERIFICATION OF A DATAFLOW PROCESSOR ARRAY

T. A. Henzinger, *X. Liu*, ***S. Qadeer*** *(shaz@eecs.berkeley.edu)*, *S. K. Rajamani* - Univ. of California, Berkeley, CA

9C.2 DISTRIBUTED SIMULATION OF VLSI SYSTEMS VIA LOOKAHEAD-FREE SELF-ADAPTIVE OPTIMISTIC AND CONSERVATIVE SYNCHRONIZATION

D. Lungeanu *(dragosl@ee.washington.edu)*, *C.-J. R. Shi* - Univ. of Washington, Seattle, WA

9C.3 SYNCHRONOUS EQUIVALENCE FOR EMBEDDED SYSTEMS: A TOOL FOR DESIGN EXPLORATION

H. Hsieh *(harry@ic.eecs.berkeley.edu)*, *A. L. Sangiovanni-Vincentelli* - Univ. of California, Berkeley, CA
F. Balarin - Cadence Berkeley Labs., Berkeley, CA
L. Lavagno - Univ. di Udine, Udine, Italy

SESSION 9D

Time: **9:00 AM to 10:30 AM** Room: **Oak**

FANOUT OPTIMIZATION

Moderators: *Yuji Kukimoto* - Monterey Design Systems, Inc., Sunnyvale, CA
Shih-Chieh Chang - National Chung-Cheng Univ., Taiwan, ROC

9D.1 ON THE GLOBAL FANOUT OPTIMIZATION PROBLEM

R. Murgai *(murgai@fla.fujitsu.com)* - Fujitsu Labs. of America, Inc., Sunnyvale, CA

9D.2 LEOPARD: A LOGICAL EFFORT-BASED FANOUT OPTIMIZER FOR AREAAND DELAY

P. Rezvani *(peyman@zugros.usc.edu)*, *A. Ajami*, *M. Pedram* - Univ. of Southern California, Los Angeles, CA
H. Savoj - Magma Design Automation, Inc., Cupertino, CA

9D.3 OPTIMUM LOADING DISPERSION FOR HIGH-SPEED TREE-TYPE DECISION CIRCUITRY

J.-H. Jiang, ***I. H.-R. Jiang*** *(huiru@cis.nctu.edu.tw)* - National Chiao Tung Univ., Taiwan, ROC

SESSION 10A

Time: **11:00 AM to 12:30 PM** Room: **Cedar**

TIMING ANALYSIS

Moderators: *David J. Hathaway* - IBM Corp., Essex Junction, VT
Joao P. Marques Silva - Technical Univ. of Lisbon, Lisboa, Portugal

10A.1 SYMBOLIC FUNCTIONAL AND TIMING VERIFICATION OF TRANSISTOR-LEVEL CIRCUITS

C. B. McDonald *(clayton@ece.cmu.edu)*, *R. E. Bryant* - Carnegie Mellon Univ., Pittsburgh, PA

10A.2 BODY-VOLTAGE ESTIMATION IN DIGITAL PD-SOI CIRCUITS AND ITS APPLICATION TO STATIC TIMING ANALYSIS

K. L. Shepard (shepard@ee.columbia.edu), ***D.-J. Kim*** - Columbia Univ., New York, NY

10A.3S FUNCTIONAL TIMING OPTIMIZATION

A. Saldanha *(saldanha@cadence.com)* - Cadence Design Systems, Inc., Berkeley, CA

10A.4S TIMING-SAFE FALSE PATH REMOVAL FOR COMBINATIONAL MODULES

Y. Kukimoto *(kukimoto@montereydesign.com)* - Monterey Design Systems, Inc., Sunnyvale, CA
R. K. Brayton - Univ. of California, Berkeley, CA

SESSION 10B

Time: **11:00 AM to 12:30 PM** Room: **Pine/Fir**

CONCURRENCY IN EMBEDDED SYSTEMS

Moderators: *Joseph Buck* - Synopsys, Inc., Mountain View, CA
Wayne Wolf - Princeton Univ., Princeton, NJ

10B.1 JMTP: AN ARCHITECTURE FOR EXPLOITING CONCURRENCY IN EMBEDDED JAVA APPLICATIONS WITH REAL-TIME CONSIDERATIONS

R. Helaihel *(rashhel@stanford.edu)*, *K. Olukotun* - Stanford Univ., Stanford, CA

10B.2 FUNSTATE—AN INTERNAL DESIGN REPRESENTATION FOR CODESIGN

L. Thiele (thiele@tik.ee.ethz.ch), *K. Strehl* - Swiss Federal Institute of Technology, Zurich, Switzerland
D. Ziegenbein, *R. Ernst* - Technical Univ. of Braunschweig, Braunschweig, Germany
J. Teich - Univ. of Paderborn, Paderborn, Germany

10B.3 FAST PERFORMANCE ANALYSIS OF BUS-BASED SYSTEM-ON-CHIP COMMUNICATION ARCHITECTURES

K. Lahiri *(klahiri@ece.ucsd.edu)*, *S. Dey* - Univ. of California at San Diego, La Jolla, CA
A. Raghunathan - NEC USA, C&C Research Labs., Princeton, NJ

SESSION 10C

Time: **11:00 Am to 12:30 PM** Room: **Donner/Siskiyou**

SEMI-FORMAL VERIFICATION

Moderators: *Thomas R. Shiple* - Synopsys, Inc., Mountain View, CA
Alan Hu - The Univ. of British Columbia, Vancouver, Canada

10C.1 PROBABILISTIC STATE SPACE SEARCH

A. Kuehlmann *(kuehl@watson.ibm.com)* - IBM Corp., Yorktown Heights, NY
K. L. McMillan - Cadence Design Systems, Inc., Berkeley, CA
R. K. Brayton - Univ. of California, Berkeley, CA

10C.2 IMPROVING COVERAGE ANALYSIS AND TEST GENERATION FOR LARGE DESIGNS

J. P. Bergmann *(bergmann@cs.stanford.edu)*,
M. A. Horowitz - Stanford Univ., Stanford, CA

10C.3 MODELING DESIGN CONSTRAINTS AND BIASING IN SIMULATION USING BDDS

J. Yuan *(ra3940@email.sps.mot.com)* - Motorola, Inc., Austin, TX
S. K. Shultz, *C. Pixley* - Motorola Inc., Austin, TX
H. Miller - Motorola Semiconductor Israel Ltd., Herzelia, Israel
A. Aziz - Univ. of Texas, Austin, TX

SESSION 10D

Time: **11:00 AM to 12:30 PM** Room: **Oak**

INTELLECTUAL PROPERTY PROTECTION

Moderators: *Emil S. Ochotta* - Xilinx, Inc., San Jose, CA
Margarida Jacome - Univ. of Texas, Austin, TX

10D.1 COPYRIGHT PROTECTION OF DESIGNS BASED ON MULTI SOURCE IPS

E. Charbon *(charbon@eecs.berkeley.edu)*, *I. Torunoglu* - Cadence Design Systems, Inc., San Jose, CA

10D.2 LOCALIZED WATERMARKING: METHODOLOGY AND APPLICATION TO OPERATION SCHEDULING

D. Kirovski *(darko@cs.ucla.edu)*, *M. Potkonjak* - Univ. of California, Los Angeles, CA

10D.3 COPY DETECTION FOR INTELLECTUAL PROPERTY PROTECTION OF VLSI DESIGNS

A. B. Kahng, *D. Kirovski*, ***S. Mantik*** (stefanus@cs.ucla.edu), *M. Potkonjak*, *J. L. Wong* - Univ. of California, Los Angeles, CA

All Speakers are denoted in bold
Email Addresses are for corresponding authors
S - denotes short paper

SESSION 11A

Time: **2:00 PM to 3:30 PM** Room: **Donner/Siskiyou**

EMBEDDED TUTORIAL - PATH TOWARD FUTURE CAD ENVIRONMENTS FOR MEMS

Moderator: *Jacob White* - Massachusetts Institute of Technology, Cambridge, MA

As MEMS technology is inserted into more and more embedded systems, the drive to lower cost will push integration of digital and analog electronics with micromechanical sensors and actuators. There is a related market push to deliver reliable MEMS from concept to product with design cycle times comparable to mixed-signal ICs. The unique requirement of MEMS to integrate electronics with mechanics, electrostatics and other physical processes translates into new challenges and opportunities for CAD. Application engineers from industry and emerging MEMS CAD vendors are beginning to successfully blend traditional electronics IC CAD concepts with new tools tailored to MEMS.

MEMS design requires simultaneous evaluation of system architecture to describe functionality, of device topology to describe geometric interactions, and of process flow to determine material properties and other mechanical characteristics. A handful of foundries now provide access to fixed MEMS processes that are capable of fabricating an important variety of systems. The foundries eliminate the need for custom process design and have motivated formation of hierarchical design methodologies and supporting representations that apply to a majority of MEMS applications and processes. Such a structured approach will lead to design reuse and core-based design of complex mixed-domain systems on a chip.

In this tutorial, we will introduce design techniques for microelectromechanical devices and systems that are compatible with VLSI design methodologies. We will describe micromechanical design tools implemented in existing frameworks having links between physical form and function. Examples of inertial sensors and micromechanical filters will be used to demonstrate a design flow consisting of mixed electrical and mechanical schematic design entry, behavioral simulation using analog HDL, micromechanical layout synthesis, extraction and verification. We will highlight design issues specific to MEMS that have driven tool development, including mixed-domain modeling, device geometry, layout position, design rules and manufacturing variations. Our goal is to overview MEMS application areas, and enable CAD engineers to understand the primary issues involved in integrating MEMS design with traditional electronics design flows.

PRESENTERS:

Gary K. Fedder - Carnegie Mellon Univ., Pittsburgh, PA
Tamal Mukherjee - Carnegie Mellon Univ., Pittsburgh, PA

SESSION 11B

Time: **2:00 PM to 3:30 PM** Room: **Pine/Fir**

ICCAD/ISSS INVITED PAPERS

Moderator: *Nikil Dutt - Univ. of California, Irvine, CA*

11B.1 INVITED TALK: DESIGN OF A SET-TOP BOX SYSTEM ON A CHIP

This presentation will review system-level issues associated with integrating the major blocks of a Set-Top Box on to a single die. In addition to the challenges of merging several powerful functions into a single chip, the goal of integration is to yield a composite design that is not only more cost effective but also provides more function than the sum of discrete parts. This is accomplished through consolidated and shared memory, improved system bandwidth and efficiency, and additional inter-macro signals to facilitate improved communication.

Eric Foster - IBM Corp., Endicott, NY

11B.2 INVITED TALK: ON THE RAPID PROTOTYPING AND DESIGN OF A WIRELESS COMMUNICATION SYSTEM ON A CHIP

The evolutionary convergence of computing, integrated circuit technology, and advances in wireless communications has led to an explosive growth of personal communication devices and services (PCS). In fact, the dramatic "Moores Law" shrinkage of IC devices, itself, has lead to an unprecedented ability to place increasingly complex systems on a chip (SoC). In a wireless communication environment, the integration task is made more difficult by the need to integrate RF, mixed signal, and digital systems. Furthermore, the digital system design task generally requires a mapping of heterogeneous stacks of software processes onto a similarly diverse collection of DSPs, uPs, and ASICs.

In this presentation, we give an overview of a modern wireless communication device and describe advanced system level design methodologies utilized for rapid prototyping and design of current and next generation systems.

Brian Kelley - Motorola, Inc., Boynton Beach, FL

SESSION 12A

Time: **4:00 PM to 5:30 PM** Room: **Donner/Siskiyou**

EMBEDDED TUTORIAL - ADVANCES IN TRANSISTOR TIMING, SIMULATION, AND OPTIMIZATION

Moderator: *Jacob White* - Massachusetts Institute of Technology, Cambridge, MA

Atransistor-level view of the circuit design has become of paramount importance for successful designs, especially in the very demanding context of high-performance microprocessor design in the deep-submicron regime. In this tutorial, such a transistor-level view will be adopted. The VLSI custom design problem will be approached from the three perspectives of transistor-level static timing analysis, fast transistor-level simulation, and transistor-level optimization process. Specifically, the first part of this tutorial will deal with the techniques used in transistor-level static timing, highlighting the differences between gate and transistor level techniques. It will also focus on how delay calculation, false path elimination and timing checks are performed at the transistor level for both combinational and sequential circuits. A fundamental ingredient of transistor-level static timing analyzers is a fast, event-driven transistor-level circuit simulator. The second part of this tutorial will present an important class of such simulators that uses simplified yet accurate transitor models. Simulators using piece-wise constant and piece-wise linear models will be described and contrasted. Methods for computing circuit sensitivities using these simulators will be covered. Finally, the third part will present some of the very recent advances in transistor-level circuit optimization. In particular, the timing-driven custom design problem will be rigorously formalized as a constrained, nonlinear optimization problem with respect to both the geometric and timing variables of the circuit. Although the resulting problems are large-scale, it will be shown how formal optimization algorithms can solve them efficiently. The tradeoffs between circuit size, device model accuracy, and algorithmic efficiency will be discussed, and generalizations of these techniques to simultaneous device and wire sizing will be considered.

PRESENTERS:

Jacob Avidan - Synopsys, Inc., Mountain View, CA
Abe Elfadel - IBM T.J. Watson Research Ctr., Yorktown Heights, NY
D. F. Wong - Univ. of Texas, Austin,TX

SESSION 12B

Time: **4:00 PM to 5:30 PM** Room: **Pine/Fir**

JOINT ICCAD/ISSS SESSION EMBEDDED TUTORIAL: EMBEDDED JAVA: TECHNIQUES AND APPLICATIONS

Moderator: *Reinaldo Bergamaschi* - IBM T. J. Watson Research Center, Yorktown Heights, NY

Java is an ideal language for developing embedded applications. However, most Java implementations and tools were designed for workstations and have limitations due to that heritage. Special tools are required to support deployment and effect better integration with target hardware. This talk will be in two parts. The first part will provide an overview of pervasive computing with a special focus on embedded Java, and describe typical applications drawn from several different market segments. The second half will delve more deeply into the architecture of an embedded Java runtime and discuss technical issues relating to dynamic compilation, optimization, and deployment.

PRESENTERS:

Brian Barry - Object Technology International Inc., Ottawa, Canada
John Duimovich - Object Technology International Inc., Ottawa, Canada

ICCAD/ISSS PANEL: SYSTEM-LEVEL DESIGN: DESIGNERS' WISH LIST VS. REALITY

Time: 6:00 PM to 7:30 PM Room: Gateway Ballroom

Moderators: *Reinaldo Bergamaschi* - IBM T.J. Watson Research Ctr., Yorktown Heights, NY
Daniel Gajski - Univ. of California, Irvine, CA

System level design has brought together a number of formidable challenges, such as methodology, software and hardware design and design automation, to name a few. More than ever, the successfull design of a system requires all these challenges to be addressed - by both the designers and the design automation tools.

Designers, better than anyone else, know what the problems are. Design automation companies claim to know how to solve them and have the products to prove it. Is this really true? Are the design automation tools really solving the hard problems or skimming over the real challenges? This panel addresses exactly that by confronting the views of distinguished designers and tools developers.

The panelists belong to two teams. The designer team will present the main problems in doing system design including verification, IP use, integration and synthesis among others, and try to show that many of the real problems are not being addressed by current tools. The tools team will explain how the tools are indeed tackling the real problems and how the designers can make the best use out of them.

The attendees can expect a very interesting, informative and technical debate. At the end, the audience will be the judge and a verdict will be passed on what the real probelms are, which ones can be solved with existing tools, and what needs to be done in the future to address the system design challenges.

Panel Members:

Michael Franz **-** Toshiba America Electronic Components, Inc., Milpitas, CA
William Lee - IBM Corp., RTP, NC
Kees Vissers - Philips Research Labs., Eindhoven, The Netherlands
Joachim Kunkel - Synopsys, Inc., Mountain View, CA
Grant Martin - Cadence Design Systems, Inc., San Jose, CA
Arkady M. Horak - Motorola Inc., Austin, TX

TUTORIAL 1

MIXED-SIGNAL ASIC DESIGN: CAD, METHODOLOGY, CASE STUDIES

Time: **9:00 to 5:00** Room: **Cedar**

Speakers:

Rob Rutenbar - Carnegie Mellon Univ., Pittsburgh, PA
Georges G.E. Gielen - Katholieke Univ. Leuven, Belgium
Jim Holmes - Texas Instruments, Dallas, TX
Frank Op't Eynde - Alcatel Microelectronics, Zaventem, Belgium
Paolo Miliozzi - Conexant Systems, Inc. Newport Beach, CA
Koen Lampaert - Conexant Systems, Inc., Newport Beach, CA

Background: Modern System-on-Chip (SoC) designs are increasingly mixed-signal designs. Unfortunately, just as deep submicron technologies have complicated the design of digital functions with issues such as the design of digital functions with issues such as practical complexity management and predictable timing closure, likewise these technologies complicate the analog subsystems on SoC designs. Since analog circuits exploit (rather than abstract away) the low-level physics of the fabrication process, they remain difficult and costly to design, validate, reuse. The desire to do hand-crafted, one-transistor-at-a-time analog design is increasingly at odds with the need for more analog design productivity, practical circuit synthesis and reuse, and reliable verification at all levels of the mixed-signal hierarchy.

This tutorial is about recent progress in tools and methodologies for complex mixed-signal designs. The ad hoc (and often, nonexistent) analog methodologies of the past will not suffice for the future. The tutorial focusses on emerging mixed-signal tools and technologies, including industrial case studies of some real flows and designs. The intended audience is CAD professionals responsible for implementing of maintaining analog- or mixed-signal tools or flows, and circuit / system designers who have to live with the resulting tools and flows.

Description: The tutorial is divided into two sessions. The morning session will overview emerging CAD ideas and methodologies for mixed-signal designs. The first section will focus on analog building blocks (e.g., amplifiers, comparators) with emphasis on circuit and physical synthesis, libraries and reuse strategies. The second section will focus on system-level, architecture-level design, with emphasis on analog behavioral modeling and power/area/noise estimation.

The afternoon session will focus on examples of industrial CAD flows and design case studies. We will discuss barriers to top-down mixed-signal design in the real world practical methodologies for complex SoC designs, industrial reuse and IP strategies and radio frequency design methodology. Case studies include data channels, a commercial ISDN chip, and a front-to-back RF IC design flow.

Our overall goal is to give the attendee a clear picture of leading-edge industrial mixed-signal design practice, and the outlook for emerging research-level tools, techniques, and methodologies.

TUTORIAL 2

MODERN PHYSICAL DESIGN: ALGORITHM, TECHNOLOGY AND METHODOLOGY

Time: **9:00 to 5:00** Room: **Pine**

Speakers:

Andrew B. Kahng - Univ. of California, Los Angeles, CA
Majid Sarrafzadeh - Northwestern Univ., Evanston, IL

Background: This tutorial will cover "the latest word" in physical chip implementation methodology and physical design (PD) algorithm technology. The target audience consists of system and circuit designers who would benefit from understanding tool capabilities in this arena, for CAD engineers (both R&D and support), for design project managers, and for academic researchers. Familiarity with basic PD methodology is assumed.

Description: The first section will briefly review implications for PD of the process technology and system design roadmaps. A convergent RTL-down chip planning and implementation methodology will be given as context for the ensuing material. Fundamental PD problem formulations and algorithms will be summarized, concentrating on latest developments in partitioning, block placement and top-level interconnect optimization, and cell-based place-and-route. We will motivate needs for incremental optimization techniques, dealing with incomplete design data, and new tool interactions and concurrent optimizations.

The second section will zero in on "upstream interactions", i.e., interactions between traditional PD and upstream floorplanning and logic synthesis. Various approaches to achieving a convergent, predictable implementation flow will be reviewed. These center around alternate methodologies for prediction/predictability and estimation, e.g., budgeting-based planning, small blocks + wireplanning, layout-driven logic synthesis, constant-delay, etc. Particular attention will be given to performance and signal integrity optimizations.

The third section will focus on interactions with parasitic estimation, delay calculation, and timing/power/SI validations. Specific requirements for tight analysis loops, and issues for data modeling, data flows, and database organization will be discussed.

The final section will describe new linkages between traditional PD and custom layout and polygon-level optimizations. Such linkages, which may soon permeate high-end ASIC methodologies, are the consequence of manufacturability and cost considerations ($/wafer, catastrophic and parametric yield, sources of manufacturing variability). Process drivers for PD (e.g., phase-shifting masks and layout density control for uniform planarization) also provide strong impetus for PD to adopt custom-on-the-fly methodology.

TUTORIAL 3

LOW VOLTAGE/LOW POWER DESIGN METHODOLOGIES AND CAD

Time: **9:00 to 5:00** Room: **Fir**

Speakers:

Farid N. Najm - Univ. of Toronto, Toronto, Canada
Anantha Chandrakasan - Massachusetts Institute of Technology, Cambridge, MA
Rajendran Panda - Motorola, Inc., Austin, TX

Background: By way of introduction, we will first briefly review the low power/low voltage problems and provide an outline of the rest of the tutorial, which will be in three parts.

Description: The first part is focused on design techniques. Several emerging technologies such as Multiple and Variable threshold CMOS enable low voltage/low power high performance computing while providing a “knob” to dynamically adjust leakage currents. The challenges in design methodologies and tools for these technologies will be discussed. In many applications, there is significant energy advantage in using an embedded power supply scheme where the voltage can be adapted based on computational demand. Rather than designing a system with a static supply to meet a specific timing constraint under worst case conditions, it is more energy efficient to allow the voltage to vary such that the timing constraints are just met at any given operating condition. The key challenges will be discussed including regulator design, circuit styles and scheduling. Trends in low-voltage library design will also be discussed and will cover logic, memory and low-swing interconnect drivers.

In the second part, we will deal with issues of power estimation and modeling. Estimation and modeling are central to any low power design methodology. After an introduction to fundamentals of power estimation, we will discuss power modeling at the gate/cell level. These models allow power analysis to be done at higher than the transistor level. Modeling and estimation at even higher levels (e.g., RTL) are key to doing early design exploration. These will be discussed next, covering both bottom-up and top-down techniques.

Finally, we will cover power/ground bus analysis and design, power optimization, and leakage power estimation and optimization. An overview of the performance, signal integrity, and electromigration reliability issues related to power distribution problems will be given. Common design styles for power distribution, and a unified methodology to design, analyze, and verify large power/ground grids will be presented with case studies. Modeling of package inductance, decoupling capacitors, and circuit parasitics to study their effect on power grid design will be discussed. Techniques to reduce power grid simulation effort, such as vector compression and static determination of worst case power demand scenario will also be considered. Combinational/sequential logic restructuring, encoding and several special design techniques for power reduction will be reviewed. Some recent transistor level and gate level optimization techniques to reduce leakage power in dual-Vt circuits will also be presented.

TUTORIAL 4

SIGNAL INTEGRITY IN HIGH PERFORMANCE DESIGN

Time: **9:00 to 5:00** Room: **Oak**

Speakers:

David Blaauw - Motorola, Inc., Austin, TX
Anirudh Devgan - IBM Corp., Austin TX
Abhijit Dharchoudhury - Intel Corp., Austin, TX

Background: This tutorial is intended to help circuit designers, CAD tool developers, and researchers gain an understanding of the problems, available analysis tools, and mitigating circuit techniques in the area of signal integrity for high performance design.

Description: As designs are reaching Giga-Hertz clock rates, designers are increasingly forced to make trade-offs between the signal integrity and performance constraints for a design. In today's high performance designs, signal integrity arises from a number of complex issues and requires careful design and analysis of the power grid, circuit structures, and high speed interconnects.

The first part of this tutorial will give an overview of different signal integrity problems in a design and will demonstrate with industrial examples how they cause functional and performance failures. Also a brief overview of circuit extraction and interconnect modeling techniques will be covered.

Next, power grid signal integrity will be addressed, including resistive voltage drops, inductive voltage drops, and power grid resonance problems. Different power grid topologies and design methodologies will be discussed and illustrated with a number of industrial examples. The analysis approach and associated fast linear solution techniques will be presented.

The third part of this tutorial will focus on signal integrity of the circuits and interconnects. We will present different analysis approaches to evaluate cross coupling noise, and charge sharing noise and to determine if it causes functional failures. Also the effect of noise on the delay of the circuit will be addressed. We will present a number of examples of failures in industrial designs and will discuss methods for correcting noise problems.

The final part of the tutorial will discuss approaches for noise avoidance and emerging signal integrity issues, specifically self and mutual inductance, bipolar and floating body effects in SOI technologies, and signal integrity problems in ultra-low voltage designs with dual Vt technologies.