

Monday, November 7, 2005

ICCAD-2005

Registration - 7:00 am - 6:00 pm (Bayshore Foyer)

Continental Breakfast - 7:00 am (Sierra/Cascade Ballroom)

Speakers' Breakfast - 7:30 am (Monterey Room)

9:00 **Opening Session & Keynote Address: *The Cell Processor: Applications, Architecture and Design in the Multicore Era***
 H. Peter Hofstee - Cell Chief Scientist and Cell Synergistic Processor Chief Architect, IBM Systems and Technology Group, Austin, TX

10:00	Coffee Break			
	Donner Ballroom	Oak Ballroom	Pine/Fir Ballroom	Cedar Ballroom
10:30	SESSION 1A	SESSION 1B	SESSION 1C	SESSION 1D
	Memory and Arithmetic Optimizations	Design Manufacturing Interaction	Detailed Placement	Digital, Analog, and RF Test
12:00	12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)			
12:30	12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)			
2:00	SESSION 2A	SESSION 2B	SESSION 2C	SESSION 2D
	Embedded Tutorial: Design Trends	Physical Design for Manufacturing	Large-Scale Layout Techniques	Novel Ideas in Logic Synthesis
3:30	Coffee Break			
4:00	SESSION 3A	SESSION 3B	SESSION 3C	SESSION 3D
	Embedded Tutorial: Design Opportunities and Challenges with Double Gated Devices	Routing and Application Specific NoC Architectures	Memory Driven Code and Architecture Optimizations	Exploiting Arithmetic Constructs in Verification
6:00	MONDAY NIGHT PANEL: <i>CHIP DESIGN IN THE NANO ERA</i> 6:15 pm - 7:15 pm (Pine/Fir Ballroom)			

ICCAD-2005

Tuesday, November 8, 2005

Registration - 7:00 am - 6:00 pm (Bayshore Foyer)

Continental Breakfast - 7:00 am (Sierra/Cascade Ballroom)

Technology Fair - 10:00 am - 6:00 pm (Gateway Foyer)

Speakers' Breakfast - 7:30 am (Monterey Room)

Donner Ballroom	Oak Ballroom	Pine/Fir Ballroom	Cedar Ballroom	
SESSION 4A				8:30
SESSION 4B				
Buffers and Voltage Islands	Sequential Circuit Optimization	Power Grid Verification	Nanoelectronics	
				10:00
Coffee Break				
SESSION 5A				10:30
SESSION 5B				
Variability in Design	Efficient Analog Design Space Exploration Techniques	Dynamic Voltage Scaling	Biochips and DNA-Based Nanofabrication	
				12:00
				12:30
12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)				
SESSION 6A				2:00
SESSION 6B				
Efficient Simulation and Synthesis Methodologies for Analog Circuits	Technology Mapping and Timing Analysis	Power Aware System Architecture and Software Optimizations	Cellular Array Architectures	
				3:30
Coffee Break				
SESSION 7A				4:00
SESSION 7B				
Variability Aware Clocking	Oscillator Analysis	Power Noise and Thermal Issues	Nanocomputing	
				6:00
ICCAD DINNER/CASINO NIGHT • 6:30 pm - 9:00 pm (Sierra/Cascade Ballroom)				

Wednesday, November 9, 2005

ICCAD-2005

Registration - 7:00 am - 6:00 pm (Bayshore Foyer) Continental Breakfast - 7:00 am (Sierra/Cascade Ballroom) Speakers' Breakfast - 7:30 am (Monterey Room)

	Donner Ballroom	Oak Ballroom	Pine/Fir Ballroom	Cedar Ballroom
	SESSION 8A	SESSION 8B	SESSION 8C	SESSION 8D
8:30	Extraction and Modeling for Interconnect Structures	Timing and Power Optimization	System-Level Variability Modeling	Routing
10:00	Coffee Break			
	SESSION 9A	SESSION 9B	SESSION 9C	SESSION 9D
10:30	New Frontiers in High-Level Synthesis	Advances in Model Order Reduction Approaches	Statistical Timing Analysis	Problem Structure in Formal Verification
12:00	Lunch Break			
12:30	Keynote: Make It Programmable, or You Won't Make It! 1:00 - 1:45 Pine/Fir Ballroom Steve Teig - President and CEO, Tabula, Inc., Santa Clara, CA			12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)
	SESSION 10A	SESSION 10B	SESSION 10C	SESSION 10D
2:00	Analytical Placement	Embedded Tutorial: Hardware and Software Design of Energy-Efficient Sensor Platforms	Improving the Accuracy of Static Timing Analysis	Embedded Tutorial: Formal Equivalence Checking
3:30	Coffee Break			
	SESSION 11A	SESSION 11B	SESSION 11C	SESSION 11D
4:00	Embedded Tutorial: Emergent Communications	Addressing Emerging Challenges for SoCs	Statistical Optimization	Making Model Checking Practical
5:30	Registration			
6:00	Registration			

See you next year! November 5 - 9, 2006

Tutorials9:00 am - 5:00 pm	Registration8:00 am - 3:00 pm
Continental Breakfast8:00 am - 9:00 am	Lunch12:00 pm - 1:30 pm

Registration Fees IEEE/ACM Member - \$380.00 Non-Member - \$480.00 Student - \$340.00

Tutorial 1 9:00 am - 12:30 pm
Characterization and Gate Modeling for 90nm and Below
Organizer: Anirudh Devgan - *Magma Design Automation, Inc., Austin, TX*
Speakers: Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*
 Shakir Abbas - *Magma Design Automation, Inc., Santa Clara, CA*
 Noel Menezes - *Intel Corp., Hillsboro, OR*

Tutorial 2 9:00 am - 12:30 pm
Package-Chip Co-Design
Organizer: Lei He - *Univ. of California, Los Angeles, CA*
Speakers: Anirudh Devgan - *Magma Design Automation, Inc., Austin, TX*
 Shauki Elassaad - *Rio Design Automation, Santa Clara, CA*

Full-Day Tutorial

Tutorial 3 9:00 am - 5:00 pm
ESL Design: Why the Time is Right and What Are the Key Enabling Technologies
Organizer: Marcello Lajolo - *NEC Labs America, Princeton, NJ*
Speakers: Wolfgang Mueller - *Paderborn Univ., Paderborn, Germany*
 Marcello Lajolo - *NEC Labs America, Princeton, NJ*
 Luca P. Carloni - *Columbia Univ., New York, NY*
 Marcello Coppola - *ST Microelectronics, Grenoble, France*
 Felice Balarin - *Cadence Berkeley Labs., Berkeley, CA*
 Tony Givargis - *Univ. of California, Irvine, CA*
 Aarti Gupta - *NEC Labs America, Princeton, NJ*

Tutorial 4 1:30 pm - 5:00 pm
Simulation Technologies and Tools for the Nano Era
Organizer: Jaijeet Roychoudhury - *Univ. of Minnesota, Minneapolis, MN*
Speakers: Laurence W. Nagel - *Omega Enterprises, Randolph, NJ*
 Yuri Sirenko - *Berkeley Design Automation, Inc. Santa Clara, CA*
 Amit Narayan - *Berkeley Design Automation, Inc. Santa Clara, CA*

Tutorial 5 1:30 pm - 5:00 pm
Yield Maximization Algorithms
Organizer: Helmut Graeb - *Technische Universitaet Muenchen, Munich, Germany*
Speakers: Peter Feldmann - *IBM TJ Watson Research Ctr., Yorktown Heights, NY*
 Helmut Graeb - *Technische Universitaet Muenchen, Munich, Germany*
 Ulf Schlichtmann - *Technische Universitaet Muenchen, Munich, Germany*