

Thursday, November 13, 2003

ICCAD-2003

Tutorials9:00 AM - 5:00 PM
Continental Breakfast8:00 AM - 9:00 AM

Registration8:00 AM - 10:00 AM
Lunch12:00 PM - 1:00 PM

Cedar Ballroom

Pine Ballroom

Tutorial 1 - Linux for EDA

Speakers: Stephen Edwards - *Columbia University, New York, NY*
Tom Grotton - *Cadence Design Systems, Inc., San Jose, CA*
Tim Marriott - *Synopsys, Inc., Santa Clara, CA*
Mel Nicholson - *Synopsys, Inc., Santa Clara, CA*
Fabio Somenzi - *Univ. of Colorado, Boulder, CO*

Over the last three years a large number of EDA tools have become available under Linux. While it is clear that the EDA industry has adopted Linux as one of the main platforms, the process of migrating applications to it has not reached maturity yet. This tutorial is therefore addressed to people involved in developing, porting, or deploying EDA software in the Linux environment. The tutorial will cover portability issues, programmer productivity tools, and performance analysis tools. The tutorial will also include a section on grid computing and the benefits and complexities of using parallel computing for CAD applications. Finally, the tutorial will include a discussion of the challenges involved in making Linux the main development platform.

The tutorial is intended for designers and CAD engineers interested in Linux as a CAD platform. Basic background in software development is useful though not needed.

Tutorial 2 - Leakage Issues in IC Design: Trends, Estimation and Avoidance

Speakers: Siva Narendra - *Intel Labs., Hillsboro, OR*
David Blaauw - *Univ of Michigan, Ann Arbor, MI*
Anirudh Devgan - *IBM Research, Austin, TX*
Farid Najm - *Univ. of Toronto, Toronto, ON, Canada*

Leakage power is emerging as a key challenge in IC design. Traditionally, leakage has been considered as an important design variable in handheld devices and in standby circuit operation. However, this significant increase of leakage now warrants that it be considered as the key design variable in all IC designs. This tutorial presents a comprehensive review of leakage power issues in IC design. The tutorial is organized in four major parts. The first part provides an overview of technology and scaling trends which are causing the significant increase in leakage current. The device physics that leads to sub-threshold and gate leakage will be described, along with their dependence on circuit design variables. The second part of the tutorial will focus on circuit level leakage estimation and avoidance. Comprehensive description of multiple-Vt techniques for leakage avoidance will be presented along with associated leakage estimation techniques. The third part of the tutorial focuses on chip level effects on leakage. Leakage estimation techniques which consider both inter and intra-die process variations will be covered as will leakage minimization techniques such as Adaptive Body Bias (ABB) and power supply control. The final part of the tutorial covers system and circuit architectures for leakage avoidance. In standby mode, the leakage of the circuit can be lowered by putting it a low-leakage state. This section of the tutorial will cover topics including state assignment for leakage minimization, leakage-driven memory and cache circuits and architectures.

The tutorial is intended for designers and CAD engineers interested in next generation design techniques and methodologies and emerging power challenges. Basic background of VLSI and CAD is useful though not needed.

Fir Ballroom

Tutorial 3 - Recent Advances in Formal Verification

Speakers: Pei-Hsin Ho - *Synopsys, Inc., Beaverton, OR*
 Ken McMillan - *Cadence Berkeley Labs., Berkeley, CA*
 Vigyan Singhal - *Jasper Design Automation, Inc., Fremont, CA*

Recent progress in model checking techniques has allowed formal verification to be applied to larger and more complex design blocks. This tutorial will examine some of the recent methods that have led to a remarkable expansion in the capacity of formal verification tools. The tutorial will be divided into three parts. The first section will discuss iterative abstraction methods. One key to verifying assertions in larger designs is to be able to automatically determine which parts of a design are relevant to a given property. In the past few years, a number of new techniques have been developed for this purpose. This has made it possible in many cases to verify assertions on designs blocks with thousands of registers. The second portion will cover the role of Boolean SAT solvers in model checking. Many recent model checking approaches make use of Boolean satisfiability solvers. We will look at how SAT solvers work, why and in what cases they can be applied effectively to large problems, and how they can be exploited in model checking. The final section will cover predicate abstraction. This approach has made it possible to apply model checking to verify properties of relatively large pieces of software, such as device drivers in the Windows and Linux kernels.

The tutorial is intended for designers and CAD engineers interested in next generation formal verification methods. Basic background of VLSI and CAD is useful though not needed.

Oak Ballroom

Tutorial 4 - Embedded Software Development

Speakers: Lance Brooks - *Mentor Graphics Corp., Mobile, AL*
 Mike McGrath - *Intel Corp., Chandler, AZ*
 Vladimir Ivanovic - *California State Univ., Hayward, CA*

Embedded software development is unlike software development for desktop or network environments. It is unique not only because every embedded device serves a unique purpose, it is different due to the very nature of firmware being very close to specialized hardware. This tutorial will provide an overview of the various pieces involved to develop embedded applications in a cross-target environment, including: integrated development environments for creating the software; compilers and associated tools for building the software targeted for various embedded CPUs and System-on-Chips (SoCs); debuggers designed to debug software running on the many different types of embedded CPU cores; and finally the different types of debug connections to various target execution environments and actual embedded hardware. The tutorial will also cover the specific problems faced by designers writing software prior to the availability of hardware. Attendees will leave with a good understanding of various pieces and the roles they play so they are better prepared to develop embedded software.

The tutorial is intended for designers and CAD engineers interested in the design of embedded software. Basic background in software development and VLSI is useful though not needed.