


Monday, November 5, 2001

ICCAD-2001

Registration - 7:00 AM - 5:00 PM (Bayshore Foyer)

Continental Breakfast - 7:00 AM (Sierra/Cascade Ballroom)

Speakers' Breakfast - 7:30 AM (Monterey Room)

8:30	OPENING SESSION: Nanotechnology and the Information Age Thomas N. Theis - Director of Physical Sciences, IBM Corp. TJ Watson Research Ctr. (Gateway Ballroom)			
9:45	Coffee Break Sponsored by: 			
	Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom
10:30	SESSION 1A	SESSION 1B	SESSION 1C	SESSION 1D
	Dynamic Verification	System-Level Exploration and Design	Interconnect Planning	Analog Macro-Modeling
12:30	12:30 - 2:00 Lunch Break (Sierra/Cascade Ballroom)			
2:00	SESSION 2A		SESSION 2B	
	Embedded Tutorial: Platform-Based Design		Embedded Tutorial: VLSI Microsystems: The Power of Many	
3:30	Coffee Break			
4:00	SESSION 3A	SESSION 3B	SESSION 3C	SESSION 3D
	Sequential Synthesis	Compiler Techniques in System Level Design	Routing Architecture and Techniques for FPGAs	Interconnect Performance & Reliability Optimization
5:30	WILL NANOTECHNOLOGY CHANGE THE WAY WE DESIGN AND VERIFY SYSTEMS?			6:00 PM - 7:30 PM (Gateway Ballroom)

ICCAD-2001

Tuesday, November 6, 2001

Registration - 7:00 AM - 5:00 PM (Bayshore Foyer)

Continental Breakfast - 7:00 AM (Sierra/Cascade Ballroom)

Speakers' Breakfast - 7:30 AM (Monterey Room)

Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom	
SESSION 4A				9:00
Circuit Structure in Formal Verification				
SESSION 4B		SESSION 4C		10:30
System Level Power and Performance Modeling		Topics in Physical Synthesis		
Model Order Reduction				11:00
Coffee Break				
SESSION 5A		SESSION 5B		12:30
Embedded Tutorial: Embedded Software and Systems		Embedded Tutorial: CAD Solutions and Outstanding Challenges for Mixed-Signal and RF IC Design		
12:30 - 2:00 Lunch Break (Sierra/Cascade Ballroom)				
SESSION 6A	SESSION 6B	SESSION 6C	SESSION 6D	2:00
BDDs and SAT	Convergence of Abstractions in High Level Synthesis	Signal Integrity and Clock Design	Analog Synthesis	
				3:30
Coffee Break				
SESSION 7A	SESSION 7B	SESSION 7C	SESSION 7D	4:00
Manufacturing Test: Stuck-At to Crosstalk	Architecture Oriented Scheduling	New Techniques in Routing	Issues in Substrate Coupling	
				5:30

Wednesday, November 7, 2001

ICCAD-2001

Registration - 7:00 AM - 5:00 PM (Bayshore Foyer)
 Speakers' Breakfast - 7:30 AM (Monterey Room)

Continental Breakfast - 7:00 AM (Sierra/Cascade Ballroom)

	Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom
8:30	SESSION 8A	SESSION 8B	SESSION 8C	SESSION 8D
	Combinational Optimization	Real Time Scheduling and Performance Analysis	Power Analysis	Timing and Noise Analysis
10:00	Coffee Break			
10:30	SESSION 9A	SESSION 9B	SESSION 9C	SESSION 9D
	System Level Test and Reliability	Power Issues in High Level Synthesis	Advances in Placement	Interconnect Analysis and Extraction
12:30	12:30 - 2:00 Lunch Break (Sierra/Cascade Ballroom)			
2:00	SESSION 10A	SESSION 10B	SESSION 10C	
	Don't Care Optimization and Boolean Matching	Power Saving Techniques for Embedded Processors	Embedded Tutorial: IC Power Distribution Challenges	
3:30	Coffee Break			
4:00	SESSION 11A			
	Panel: Automatic Hierarchical Design: Fantasy or Reality?			
5:30				

Tutorials	9:00 AM - 5:00 PM	Registration	8:00 AM - 10:00 AM
Continental Breakfast	8:00 AM - 9:00 AM	Lunch	12:00 PM - 1:00 PM

Tutorial 1 - Electrical-Integrity Design and Verification for Digital and Mixed-Signal Systems-On-A-Chip Cedar Ballroom
 Speakers: Dennis Sylvester - Univ. of Michigan, Ann Arbor, MI
 Kenneth L. Shepard - Columbia Univ., New York, NY

Tutorial 2 - Boolean Satisfiability Solving and its Application in Equivalence and Model Checking Pine Ballroom
 Speakers: Joao Marques-Silva - Tech. Univ. of Lisbon, Lisboa, Portugal
 Per Bjesse - Prover Tech., Portland, OR
 Wolfgang Kunz - Univ. of Frankfurt, Frankfurt, Germany

Tutorial 3 - Optimization Strategies for Physical Synthesis and Timing Closure Oak Ballroom
 Speakers: Charles J. Alpert - IBM Corp., Austin, TX
 Sachin S. Sapatnekar - Univ. of Minnesota, Minneapolis, MN
 Salil Raje - Monterey Design Systems, Inc., Sunnyvale, CA

Keynote: Nanotechnology and the Information Age

Thomas N. Theis - Director, Physical Sciences, IBM Corp. TJ Watson Research Ctr., Yorktown Heights, NY

8:30 AM - 9:45 AM in the Gateway Ballroom

The history of information technology can be viewed as a quest to make "bits" smaller and smaller. There is no obvious and hard physical limit to the minimum size of logical devices that process information or the marks that store information. Indeed, quantum physics is being recast as a theory of information, and even a single atom can no longer be seen as the ultimate limit to the minimum size of a bit. Yet the smallest logical devices being manufactured today contain billions of atoms, and the smallest magnetic bits on commercial hard drives contain millions of atoms. Optimistically assuming continued exponential improvement in our ability to pattern matter at ever-smaller dimensions, in perhaps 35 years we will have the capability to design and control the structure of an object on all length scales from the atomic to the macroscopic -- in other words, the beginnings of a mature nanotechnology. Progress along this road will depend not only on the continued extension of lithographic patterning

techniques, but on increasing use of processes of natural pattern formation, commonly referred to as self-assembly. Continued evolutionary progress in silicon microelectronics and magnetic storage seems assured for at least another decade. Potential nanoscale successors, such as scanning-probe storage and carbon-nanotube electronics are under active investigation and suggest the possibility of continued exponential progress in information technology for decades to come.

Biography: Thomas Theis received the B.S. degree in physics from Rensselaer Polytechnic Institute in 1972, and M.S. and Ph.D. degrees from Brown University in 1974 and 1978, respectively. A portion of his Ph.D. research was done at the Technical University of Munich, where he completed a postdoctoral year before joining IBM Research in 1979.

Time: 10:30 AM to 12:00 PM

Room: Cedar

SESSION 1A DYNAMIC VERIFICATION

Moderators: Jay Lawrence - Cadence Design Systems, Inc.,
Chelmsford, MA
Kunle Olokotun - Stanford Univ., Stanford, CA

This session explores techniques in high performance dynamic verification. Two approaches to verifying memory access in multi-processor based systems are shown. In addition, a theory of when parallel simulation may be profitably applied is shown.

1A.1 STATIC SCHEDULING OF MULTI-DOMAIN MEMORIES FOR FUNCTIONAL VERIFICATION

Murali Kudlugi, Charles Selvidge - IKOS Systems Inc.,
Waltham, MA
Russell Tessier (tessier@ecs.umass.edu) - Univ. of
Massachusetts, Amherst, MA

1A.2 A SIMULATION-BASED METHOD FOR VERIFICATION OF SHARED MEMORY IN MULTIPROCESSOR SYSTEMS

Scott A. Taylor (Scott.Taylor@compaq.com) - Intel Corp.,
Shrewsbury, MA
Carl Ramey - Stargen, Inc., Marlborough, MA
Craig Barner, David Asher - Cavium Networks, Marlborough, MA

1A.3 PREDICTING THE PERFORMANCE OF SYNCHRONOUS DISCRETE EVENT SIMULATION SYSTEMS

Jinsheng Xu (xujinshe@pilot.msu.edu), Moon Jung Chung -
Michigan State Univ., East Lansing, MI

Time: 10:30 AM to 12:00 PM

Room: Pine/Fir

SESSION 1B SYSTEM-LEVEL EXPLORATION AND DESIGN

Moderators: Yanbing Li - Synopsys, Inc., Mountain View, CA
Xiaobo (Sharon) Hu - Univ. of Notre Dame,
Notre Dame, IN

Exploring the range of system architectures and mappings of applications to architectures is needed to achieve efficient embedded system implementations. The first paper describes techniques for exploring the space of possible configurations for a parameterized architecture. The second paper provides a case study exploring JPEG encoder using the SPADE methodology. The third paper introduces a suite of benchmarks for networking, which can be used to drive architecture design.

1B.1 SYSTEM-LEVEL EXPLORATION FOR PARETO-OPTIMAL CONFIGURATIONS IN PARAMETERIZED SYSTEM-ON-A-CHIP

Tony D. Givargis (givargis@cs.ucr.edu) - Univ. of California,
Irvine, CA
Frank Vahid - Univ. of California, Riverside, CA
Joerg Henkel - NEC Corp., Princeton, NJ

1B.2 SYSTEM LEVEL DESIGN WITH SPADE: AN M-JPEG CASE STUDY

Paul Lieveise (p.lieveise@its.tudelft.nl) - Delft Univ. of Tech.,
Delft, The Netherlands
Todor Stefanov - Leiden Univ., Leiden, The Netherlands
Pieter van der Wolf - Philips Research Labs., Eindhoven, The
Netherlands
Ed Deprettere - Leiden Univ., Leiden, The Netherlands

1B.3 NETBENCH: A BENCHMARKING SUITE FOR NETWORK PROCESSORS

Gokhan Memik, Bill Mangione-Smith (billms@ee.ucla.edu),
Wendong Hu - Univ. of California, Los Angeles, CA

Time: 10:30 AM to 12:30 PM

Room: Donner/Siskiyou

SESSION 1C INTERCONNECT PLANNING

Moderators: Robi Dutta - Synopsys, Inc., Mountain View, CA
 Chung-Kuan Cheng - Univ. of California at San Diego,
 La Jolla, CA

This session presents new work in interconnect planning. The first paper examines the effects of thermal gradients on buffer insertion strategies. The second paper presents a new algorithm for buffer tree synthesis. The third paper introduces novel encoding strategies for avoidance of crosstalk-induced delay in global buses.

1C.1 ANALYSIS OF SUBSTRATE THERMAL GRADIENT EFFECTS ON OPTIMAL BUFFER INSERTION

Amir H. Ajami (ajami@scf.usc.edu) - Univ. of Southern California, Los Angeles, CA
 Kaustav Banerjee - Stanford Univ., Stanford, CA
 Massoud Pedram - Univ. of Southern California, Los Angeles, CA

1C.2 A NEW ALGORITHM FOR ROUTING TREE CONSTRUCTION WITH BUFFER INSERTION AND WIRE SIZING UNDER OBSTACLE CONSTRAINTS

Xiaoping Tang (tang@cs.utexas.edu), Ruiqi Tian, D.F. Wong, Hua Xiang - Univ. of Texas, Austin, TX

1C.3 BUS ENCODING TO PREVENT CROSSTALK DELAY

Bret Victor (bret@eecs.berkeley.edu), Kurt Keutzer - Univ. of California, Berkeley, CA

Time: 10:30 AM to 12:30 PM

Room: Oak

SESSION 1D ANALOG MACROMODELING

Moderators: Rob A. Rutenbar - Carnegie Mellon Univ., Pittsburgh, PA
 Henry Chang - Cadence Design Systems, Inc., San Jose, CA

Macromodeling techniques reduce the behavior of very large or very nonlinear systems to simpler models we can simulate and optimize efficiently. The first two papers in this session offer new analog circuit modeling methods based on wavelet and signomial/posynomial representation respectively. The final paper gives new techniques for fast power grid transient simulation.

1D.1 BEHAVIORAL MODELING OF ANALOG CIRCUITS BY WAVELET COLLOCATION METHOD

Xin Li (xinli@fudan.edu), Xuan Zeng - Fudan Univ., Shanghai, China
 Dian Zhou - Univ. of Texas, Richardson, TX
 Xieting Ling - Fudan Univ., Shanghai, China

1D.2 SIMULATION-BASED AUTOMATIC GENERATION OF SIGNOMIAL AND POSYNOMIAL PERFORMANCE MODELS FOR ANALOG INTEGRATED CIRCUITS

Walter Daems (Walter.Daems@esat.kuleuven.ac.be), Georges Gielen, Willy Sansen - Katholieke Univ., Leuven, Belgium

1D.3 POWER GRID TRANSIENT SIMULATION IN LINEAR TIME BASED ON TRANSMISSION-LINE-MODELING ALTERNATING-DIRECTION-IMPLICIT METHOD

Yu Min Lee (yu-min@cae.wisc.edu), Chung Ping Chen - Univ. of Wisconsin, Madison, WI

Monday, November 5, 2001

ICCAD-2001

Time: 2:00 PM to 3:30 PM

Room: Cedar

SESSION 2A EMBEDDED TUTORIAL:
PLATFORM-BASED DESIGNS

Moderator: Ellen M. Sentovich - Cadence Berkeley Labs.,
Berkeley, CA

This embedded tutorial is divided into three parts. The first part is an overview of the philosophy and research directions for platform-based design, and the second and third parts relate the experience of a platform designer and user.

The system-on-a-chip (SoC) dream has not yet come true. As chip sizes grow, so do their manufacturing costs and NRE costs, while design productivity drops due to the increased complexity. Platform-based design promises to change this by offering a design style in which systems can be assembled quickly from pre-designed and pre-characterized components. This design flow can be integrated with a traditional custom flow to obtain an overall design style with an appropriate mix of flexible, re-usable, easy-to-integrate parts, and optimized custom parts. The first part of this tutorial will outline the entire system-to-silicon platform-based flow.

The second part of this tutorial will be given from the perspective of a platform designer. Philips has invested heavily in a platform, Nexperia, for multi-media applications. The platform consists of a hardware platform and a software platform. The hardware platform consists of two processors, a VLIW processor and a MIPS micro-processor, and of appropriate memory, interconnection and peripherals. The software platform is quite articulated including APIs, compilers, high-level primitives, and support for a variety of RTOS, such as VXworks, Windows CE and Linux. The critical decisions that led to the Nexperia solution will be reviewed and then some examples of applications will be given.

The final part of this tutorial will be given from the perspective of a platform user. BMW has been the fastest automotive company to recognize the value of advanced system level design. In particular, BMW has been focusing on the difficult task of integrating different components for the electronics systems in the car. In this domain, platform-based design and its associated paradigms seem to work well, thus saving costs and development times. In this tutorial, the BMW experience in using the system level design methodology based on platforms will be reported and issues related to its application will be presented.

Presenters: Alberto L. Sangiovanni-Vincentelli - Univ. of California
and Cadence Design Systems, Berkeley, CA
Augusto de Oliveira - Philips Semiconductor,
Sunnyvale, CA
Thilo Demmeler - BMW Technology Office,
Palo Alto, CA

Time: 2:00 PM to 3:30 PM

Room: Cedar

SESSION 2B EMBEDDED TUTORIAL: VLSI
MICROSYSTEMS: THE POWER OF MANY

Moderator: Matton Kamon - Conventor, Inc., Cambridge, MA

As information systems increasingly leave fixed locations and appear in our pockets and palms, they are getting closer to the physical world, creating new opportunities for perceiving and controlling our machines, structures and environments. MEMS is a revolutionary enabling technology that merges computation and communication with sensing and actuation to change the way people and machines interact with the physical world. Using the same fabrication processes and materials that are used to make microelectronic devices, MEMS conveys the advantages of miniaturization, multiple components, and integrated microelectronics to the design and construction of integrated electromechanical systems. Widespread applications of MEMS include: miniature inertial measurement units for personal navigation, mass data storage devices, miniature analytical instruments, fiber-optic network switches, displays, electromechanical signal processing, on demand structural strength and distributed/unattended sensors for process, system and environmental monitoring.

The future promise of MEMS will be in our ability to design systems of components with thousands to millions of electromechanical parts integrated with electronics to create MEMS arrays that have a systems function greater than the sum of the individual parts. This next stage in the evolution and maturity of MEMS will be driven less by captive fabrication facilities and process development and more by

innovative, aggressive and integrated multi-technology systems designs. Central to our ability to create these kinds of systems are CAD tools that can capture and integrate the multiple technologies and yet retain the hierarchical, cell-based capabilities of today's microelectronics CAD tools. MEMS is poised to take full advantage of advances in information technology and couple them to advances in related microsystems technology to drive a fundamentally new approach to electromechanical system design and fabrication. For the first time, approaches akin to VLSI electronics can be taken to usher in an equally exciting and productive era of VLSI Microsystems.

Presenters: Kaigham J. Gabriel - Carnegie Mellon Univ.,
Pittsburgh, PA
Mary-Ann Maher- MEMSCAP, Inc., Oakland, CA

Time: 4:00 PM to 5:30 PM

Room: Cedar

SESSION 3A SEQUENTIAL SYNTHESIS

Moderators: Hamid Savoj - Magma Design Automation, Inc.,
Cupertino, CA

Diana Marculescu - Carnegie Mellon Univ., Pittsburgh, PA

This session begins with a talk on extending the motion of SPFD's to sequential circuits and using them for sequential synthesis. The next two talks are related to retiming problems, one from a more theoretical standpoint and one that deals with practical issues. The final paper in the session presents a theoretical framework for the composition of finite state machines.

3A.1 SEQUENTIAL SPFDs

Subarnarekha Sinha (subarna@eecs.berkeley.edu) - Univ. of California, Berkeley, CA

Andreas Kuehlmann - Cadence Berkeley Labs., Berkeley, CA
Robert K. Brayton - Univ. of California, Berkeley, CA

3A.2 ON THE OPTIMIZATION POWER OF REDUNDANCY ADDITION AND REMOVAL TECHNIQUES FOR SEQUENTIAL CIRCUITS

Enrique San Millán (quique@ing.uc3m.es), Luis Entrena, Jos Alberto Espejo - Univ. Carlos III de Madrid, Leganes, Spain

3A.3 PLACEMENT DRIVEN RETIMING WITH A COUPLED EDGE TIMING MODEL

Ingmar Neumann (ineumann@em.informatik.uni-frankfurt.de), Wolfgang Kunz - Univ. of Frankfurt, Frankfurt, Germany

3A.4 SOLUTION OF PARALLEL LANGUAGE EQUATIONS FOR LOGIC SYNTHESIS

Nina Yevtushenko - Tomsk State Univ., Tomsk, Russia
Tiziano Villa (villa@parades.rm.cnr.it) - Parades Labs., Rome, Italy
Robert K. Brayton - Univ. of California, Berkeley, CA
Alex Petrenko - CRIM, Montreal, PQ, Canada
Alberto L. Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA

Time: 4:00 PM to 5:30 PM

Room: Pine/Fir

SESSION 3B COMPILER TECHNIQUES IN SYSTEM LEVEL DESIGN

Moderators: Radu Marculescu - Carnegie Mellon Univ.,
Pittsburgh, PA

Grant Martin - Cadence Design Systems, Inc.,
San Jose, CA

Software compilers play a very important role in modern embedded systems design. The first paper demonstrates a software pipelining algorithm for clustered VLIW processors that can be used effectively by embedded system designers to explore different code optimization alternatives. The second paper deals with the problem of improving cache predictability and performance in embedded systems through the use of software-assisted replacement mechanisms. The third paper presents simultaneous template generation and matching for compiler instruction generation and selection for hybrid reconfigurable systems.

3B.1 CALIBER: A SOFTWARE PIPELINING ALGORITHM FOR CLUSTERED EMBEDDED VLIW PROCESSORS

Cagdas Akturan, Margarida F. Jacome
(jacome@ece.utexas.edu) - Univ. of Texas, Austin, TX

3B.2 SOFTWARE-ASSISTED CACHE REPLACEMENT MECHANISMS FOR EMBEDDED SYSTEMS

Prabhat Jain (prabhat@caa.lcs.mit.edu), Srinivas Devadas,
Daniel Engels, Larry Rudolph - Massachusetts Institute of
Tech., Cambridge, MA

3B.3 INSTRUCTION GENERATION FOR HYBRID RECONFIGURABLE SYSTEMS

Ryan Kastner (kastner@cs.ucla.edu), Seda Ogrenci Memik,
Elaheh Bozorgzadeh, Majid Sarrafzadeh - Univ. of California,
Los Angeles, CA

Time: 4:00 PM to 5:30 PM

Room: Donner/Siskiyou

**SESSION 3C ROUTING ARCHITECTURE AND
TECHNIQUES FOR FPGAS**

Moderators: Majid Sarrafzadeh - Univ. of California, Los Angeles, CA
Rajeev Jayaraman - Xilinx, Inc., San Jose, CA

This session starts with a discussion on the impact of FPGA placement on routability. It is followed by a paper on routing estimation and a paper on Incremental (ECO) routing.

**3C.1 INTERCONNECT RESOURCE AWARE PLACEMENT FOR
HIERARCHICAL FPGAS**

Amit Singh (asingh@guitar.ece.ucsb.edu), Ganapathy Parthasarathy, Malgorzata Marek-Sadowska - Univ. of California, Santa Barbara, CA

**3C.2 A ROUTER FOR SYMMETRICAL FPGAS BASED ON EXACT ROUTING
DENSITY EVALUATION**

Nak Woong Eum - ETRI, Taejon, Korea
Taewhan Kim (tkim@cs.kaist.ac.kr), Chong Min Kyung - KAIST, Taejon, Korea

**3C.3 A SEARCH-BASED BUMP AND REFIT APPROACH
TO INCREMENTAL ROUTING FOR ECO
APPLICATIONS IN FPGAS**

Vinay Verma, Shantanu S. Dutt (dutt@eecs.uic.edu) - Univ. of Illinois, Chicago, IL

Time: 4:00 PM to 5:30 PM

Room: Oak

**SESSION 3D INTERCONNECT PERFORMANCE AND
RELIABILITY OPTIMIZATION**

Moderators: David D. Ling - IBM Corp. TJ Watson Research Ctr., Yorktown Heights, NY
Ken Kundert - Cadence Design Systems, Inc., San Jose, CA

Performance and reliability constraints for chip-scale interconnect are increasingly critical to the success of any chip implementation. This session describes new optimization techniques for power grid sizing, and new modeling and simulation methods for electromigration and electrothermal effects in large-scale interconnect.

**3D.1 AREA MINIMIZATION OF POWER DISTRIBUTION NETWORK USING
EFFICIENT NONLINEAR PROGRAMMING TECHNIQUES**

Xiaohai Wu (wuxh@tiger.cs.tsinghua.edu.cn), Xianlong Hong, Yici Cai - National Tsing-Hua Univ., Beijing, China
C.K. Cheng - Univ. of California at San Diego, La Jolla, CA
Jun Gu - Univ. of Hong Kong, Hong Kong
Wayne Dai - Univ. of California, Santa Cruz, CA

**3D.2 COUPLED ANALYSIS OF ELECTROMIGRATION RELIABILITY AND
PERFORMANCE IN ULSI SIGNAL NETS**

Kaustav Banerjee (kaustav@stanford.edu) - Stanford Univ., Stanford, CA
Amit Mehrotra - Univ. of Illinois, Urbana, IL

**3D.3 COMPACT MODELING AND SPICE-BASED SIMULATION FOR
ELECTROTHERMAL ANALYSIS OF MULTILEVEL
VLSI INTERCONNECTS**

TingYen Chiang (tychiang@leland.stanford.edu), Kaustav Banerjee, Krishna C. Saraswat - Stanford Univ., Stanford, CA

Monday, November 5, 2001

ICCAD-2001

Time: 6:00 PM to 7:30 PM

Room: Gateway Ballroom

MONDAY NIGHT PANEL WILL NANOTECHNOLOGY CHANGE THE WAY WE
DESIGN AND VERIFY SYSTEMS?

Moderator: Andreas Kuehlmann - Cadence Berkeley Labs., Berkeley, CA

During the past few decades advances in semiconductor technology have had only modest implications for the design and verification of integrated systems. While "deep-submicron" effects created new challenges for guaranteeing electrical integrity and necessitated the bundling of traditionally separated design steps such as logic synthesis and physical layout, the general integrated circuit design flow did not change. But what will happen when semiconductor technology hits the wall? Which of the currently futuristic nanotechnologies will step in and how will they change the way we design and verify systems? Will we just replace the implementation of the NAND-gate and D-flipflop and then do business as usual? Or do these technologies force us to abandon convenient hierarchical modeling of electrical, logical, and system levels? The panel will discuss the exciting opportunities of nanotechnologies and their implication for the design and verification of future systems.

Panelists:

Robert W. Dutton - Stanford Univ., Stanford, CA
Paul Franzon - North Carolina State Univ., Raleigh, NC
Seth C. Goldstein - Carnegie Mellon Univ., Pittsburgh, PA
Philip Kuekes - Hewlett Packard Labs., Palo Alto, CA
Eric Parker - Zyvex, Richardson, TX
Thomas N. Theis - IBM Corp. TJ Watson Research Ctr., Yorktown Heights, NY

Time: 8:30 AM to 10:00 AM

Room: Cedar

SESSION 4A CIRCUIT STRUCTURE IN FORMAL VERIFICATION

Moderators: Masahiro Fujita - Univ. of Tokyo, Tokyo, Japan
Vigyan Singal - Tempus Fujit, Berkeley, CA

Considering specific circuit structures can greatly enhance formal verification. The first paper in the session improves min-area retiming by employing simultaneous logic optimization. The other two papers project two different efficient means to improve the verification of combinational multipliers.

4A.1 MIN-AREA RETIMING ON FLEXIBLE CIRCUIT STRUCTURES

Jason Baumgartner (jasonb@austin.ibm.com) - IBM Corp., Austin, TX
Andreas Kuehlmann - Cadence Berkeley Labs., Berkeley, CA

4A.2 VERIFICATION OF INTEGER MULTIPLIERS ON THE ARITHMETIC BIT LEVEL

Dominik A. Stoffel (stoffel@em.informatik.uni-frankfurt.de), Wolfgang Kunz - Univ. of Frankfurt, Frankfurt, Germany

4A.3 INDUCTION-BASED GATE-LEVEL VERIFICATION OF MULTIPLIERS

Ying-Tsai Chang (ytchang@bigbend.ece.ucsb.edu), Kwang-Ting (Tim) Cheng - Univ. of California, Santa Barbara, CA

PERFORMANCE MODELING

Moderators: Wayne Wolf - Mediaworks Tech., Schaumburg, IL
Preeti Panda - Synopsys, Inc., Mountain View, CA

Accurate modeling of timing performance and energy consumption are critical to effective system level architectural exploration. This task is complicated by the difficulties in software performance estimation and functional uncertainties. The first paper in this session presents an analytic model to estimate instruction level delays. The second paper presents software optimization techniques to improve energy consumption. The last paper presents a stochastic model that is useful in performance analysis of complex multimedia applications.

4B.1 AN ASSEMBLY-LEVEL EXECUTION-TIME MODEL FOR PIPELINED ARCHITECTURES

Giovanni Beltrame - CEFRIEL, Milano, Italy
Carlo Brandolese, William Fornaciari (fornacia@elet.polimi.it), Fabio Salice, Donatella Sciuto, Vito Trianni - Politecnico di Milano, Milano, Italy

4B.2 IMPROVING MEMORY ENERGY USING ACCESS PATTERN CLASSIFICATION

Mahut T. Kandemir (kandemir@cse.psu.edu) - Penn State Univ., University Park, PA
Ugur Sezer - Univ. of Wisconsin, Madison, WI
Victor Delaluz - Penn State Univ., University Park, PA

4B.3 SYSTEM-LEVEL POWER/PERFORMANCE ANALYSIS OF PORTABLE MULTIMEDIA SYSTEMS COMMUNICATING OVER WIRELESS CHANNELS

Amit Nandi, Radu Marculescu (radum@ece.cmu.edu) - Carnegie Mellon Univ., Pittsburgh, PA
Luciano Lavagno - Univ. di Udine, Udine, Italy
Alberto Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA

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Time: 8:30 AM to 10:00 AM

Room: Pine/Fir

SESSION 4B SYSTEM LEVEL POWER AND

Time: 8:30 AM to 10:00 AM

Room: Donner/Siskiyou

SESSION 4C TOPICS IN PHYSICAL SYNTHESIS

Moderators: Andrew B. Kahng - Univ. of California at San Diego, La Jolla, CA
 Malgorzata Marek-Sadowska - Univ. of California, Santa Barbara, CA

This session presents recent work on the interface of logic synthesis, layout and chip assembly. The first paper proposes novel algorithms to confirm physical layout information with early logic synthesis. The second paper addresses the problem of integrating logic synthesis and global placement for timing closure. The third paper presents a polynomial-time exact algorithm for simultaneous pin assignment and routing for 2-pin nets from the same source block to all other cells.

4C.1 CONGESTION AWARE LAYOUT
 DRIVEN LOGIC SYNTHESIS

Thomas Kutzschebauch (kutzsche@watson.ibm.com), Leon Stok - IBM Corp., Yorktown Heights, NY

4C.2 ADDRESSING THE TIMING CLOSURE PROBLEM BY INTEGRATING
 LOGIC OPTIMIZATION AND PLACEMENT

Wilsin Gosti - Univ. of California, Berkeley, CA
 Sunil Khatri (spkhatri@colorado.edu) - Univ. of Colorado, Boulder, CO
 Alberto Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA

4C.3 AN ALGORITHM FOR SIMULTANEOUS PIN
 ASSIGNMENT AND ROUTING

Hua Xiang (xiangh@cs.utexas.edu), Xiaoping Tang, D.F. Wong - Univ. of Texas, Austin, TX

Time: 8:30 AM to 10:00 AM

Room: Oak

SESSION 4D MODEL ORDER REDUCTION

Moderators: Eli Chiprout - Intel Corp., Chandler, AZ
 Andreas C. Cangellaris - Univ. of Illinois, Urbana, IL

Reducing large simulation models continues to be a concern. The first paper describes a passive and stable reduction of measured data. The second paper gives a way to reduce models that include dielectrics. The last paper describes a technique to reduce nonlinear systems.

4D.1 TECHNIQUES FOR INCLUDING DIELECTRICS WHEN EXTRACTING
 LOW-ORDER MODELS OF HIGH SPEED INTERCONNECT

Luca Daniel (dluca@eecs.berkeley.edu), Alberto Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA
 Jacob K. White - Massachusetts Institute of Tech., Cambridge, MA

4D.2 A CONVEX PROGRAMMING APPROACH TO
 POSITIVE REAL RATIONAL APPROXIMATION

Carlos Coelho - Technical Univ. of Lisbon, Lisboa, Portugal
 Joel R. Phillips - Cadence Design Systems, Inc., San Jose, CA
 Luis M. Silveira (lms@inesc.pt) - Technical Univ. of Lisbon, Lisboa, Portugal

4D.3 A TRAJECTORY PIECEWISE-LINEAR APPROACH TO MODEL ORDER
 REDUCTION AND FAST SIMULATION OF NONLINEAR CIRCUITS
 AND MICROMACHINED DEVICES

Michal Rewienski (mrewiens@mit.edu), Jacob K. White - Massachusetts Institute of Tech., Cambridge, MA

Time: 11:00 PM to 12:30 PM

Room: Cedar

SESSION 5A EMBEDDED TUTORIAL: EMBEDDED SOFTWARE AND SYSTEMS

Moderators: Rolf Ernst - Tech. Univ. of Braunschweig,
Braunschweig, Germany
Francky Catthoor - IMEC, Leuven, Belgium

The design of embedded systems is driven by conflicting optimization issues such as low power, performance, memory size and cost constraints. These stringent requirements require exploitation of domain specific knowledge at various levels of the design process. Leading researchers in the field will elaborate upon embedded system design and optimization with emphasis on system level design representations and optimization.

Modern embedded computing systems tend to be heterogeneous assemblages of concurrent subsystems, typically described in different languages and semantics. Approaches will be described which allow for the common representation of different languages and incomplete specifications. As an example, design space exploration and scheduling of network processors will be discussed.

Following the inter-component optimization aspects, software generation from higher level models will be tackled. Temporal properties are often a critical part of subsystem interaction. An approach for modeling and model compilation to generate embedded software will be described, including domain-specific and domain-independent optimizations. It exploits properties of the concurrent model of computation and supports pertinent and modal models.

A critical bottleneck in many novel multi-media applications is their very dynamic behavior due to run-time creation and deletion of tasks and complex data types, especially in the presence of quality-of-service aspects. Formal synthesis and optimization problems for dynamic concurrent task-based systems will be explained. The concept of Pareto curve based exploration is crucial to these formulations.

Finally, low power system scheduling and synthesis techniques will be surveyed including scheduling techniques for dynamic voltage scaling and dynamic power management, as well as low power system synthesis techniques for real-time distributed embedded systems. We will point out open problems which exist at the intersection of low power system scheduling and low power system synthesis.

Presenters: Niraj K. Jha - Princeton Univ., Princeton, NJ
Edward Lee - Univ. of California, Berkeley, CA
Lothar Thiele - ETH, Zurich, Switzerland
Diederik Verkest - IMEC, Leuven, Belgium

Time: 11:00 PM to 12:30 PM

Room: Donner/Siskiyou

**SESSION 5B EMBEDDED TUTORIAL: CAD SOLUTIONS
AND OUTSTANDING CHALLENGES FOR MIXED-SIGNAL
AND RF IC DESIGN**

Moderator: Georges Gielen - Katholieke Univ., Leuven, Belgium

The growth of wireless services and other telecom applications increases the need for low-cost highly integrated solutions with very demanding performance specifications. This requires the development of intelligent front-end architectures that circumvent the physical limitations posed by the technology.

In addition, with the evolution towards ultra deep submicron CMOS technologies, the design of complex systems-on-a-chip (SoC) will emerge which are increasingly mixed-signal designs, embedding high-performance analog blocks and possibly sensitive RF frontends together with complex digital circuitry on the same chip.

This embedded tutorial will address the problems and solutions that are posed by the design of such mixed-signal integrated systems. These include problems in design methodologies and flows, design

productivity, design, modeling and verification tools. The presenters will explain the problems that are posed by these mixed-signal/RF SoC designs, they will describe the solutions and their underlying methods that already exist today and outline the challenges that still remain to be solved today. The first part of the tutorial addresses the design of analog and mixed-signal circuits, the second part of the tutorial focuses on the specific problems raised by RF wireless circuits.

Presenters: Rob A. Rutenbar - Carnegie Mellon Univ., Pittsburgh, PA
Domine Leenaerts - Philips Research Labs., Eindhoven,
The Netherlands

Time: 2:00 PM to 3:30 PM

Room: Cedar

SESSION 6A BDDS AND SAT

Moderators: Alan J. Hu - Univ. of British Columbia, Vancouver, BC, Canada
Rajeev Ranjan - Real Intent, Santa Clara, CA

BDDs and SAT form the main computation engines underlying formal verification methods. This session explores techniques to make them more efficient for image computation and dynamic learning.

6A.1 EFFICIENT LEARNING IN BOOLEAN SATISFIABILITY SOLVER

Lintao Zhang (lintaoz@ee.princeton.edu), Sharad Malik - Princeton Univ., Princeton, NJ
Matthew Moskewicz - Univ. of California, Berkeley, CA
Conor Madigan - Massachusetts Institute of Tech., Boston, MA

6A.2 PARTITION-BASED DECISION HEURISTICS FOR IMAGE COMPUTATION USING SAT AND BDDS

Aarti Gupta (agupta@nec-lab.com), Zijiang Yang, Pranav N. Ashar - NEC Corp., Princeton, NJ
Lintao Zhang, Sharad Malik - Princeton Univ., Princeton, NJ

6A.3 NON-LINEAR QUANTIFICATION SCHEDULING IN IMAGE COMPUTATION

Pankajkumar P. Chauhan (pchauhan@cs.cmu.edu), Edmund M. Clarke - Carnegie Mellon Univ., Pittsburgh, PA
Somesh Jha - Univ. of Wisconsin, Madison, WI
James Kukula, Tom Shiple - Synopsys, Inc., Beaverton, OR
Helmut Veith - Technical Univ. of Vienna, Wien, Austria
Dong Wang - Carnegie Mellon Univ., Pittsburgh, PA

Time: 2:00 PM to 3:30 PM

Room: Pine/Fir

SESSION 6B CONVERGENCE OF ABSTRACTIONS IN HIGH-LEVEL SYNTHESIS

Moderators: Sandeep Shukla - Univ. of California, Irvine, CA
Francky Catthoor - IMEC, Leuven, Belgium

This session presents papers on high-level synthesis that take advantage of specific abstraction and modeling techniques. The first paper uses symbolic algebra for data-flow synthesis. The second paper models the system microarchitecture for power analysis. The third paper describes a synthesis system from matlab, and the fourth paper presents a placement-driven RTL synthesis system.

6B.1 SYMBOLIC ALGEBRA AND TIMING DRIVEN DATA-FLOW SYNTHESIS

Armita Peymandoust (armita@stanford.edu), Giovanni De Micheli - Stanford Univ., Stanford, CA

6B.2 APPLICATION-DRIVEN PROCESSOR DESIGN EXPLORATION FOR POWER-PERFORMANCE TRADE-OFF ANALYSIS

Diana Marculescu (dianam@ece.cmu.edu), Anoop Iyer - Carnegie Mellon Univ., Pittsburgh, PA

6B.3 A SYSTEM FOR SYNTHESIZING OPTIMIZED FPGA HARDWARE FROM MATLAB

Malay Haldar (malay@ece.nwu.edu) - Northwestern Univ., Evanston, IL

6B.4 BEHAVIOR-TO-PLACED RTL SYNTHESIS WITH PERFORMANCE-DRIVEN PLACEMENT

Daehong Kim (daehong@poppy.snu.ac.kr), Jinyong Jung, Sunghyun Lee - Seoul National Univ., Seoul, Korea
Jinhwan Jeon - GCT Semiconductor, Inc., Seoul, Korea
Kiyong Choi - Seoul National Univ., Seoul, Korea

Time: 2:00 PM to 3:30 PM

Room: Donner/Siskiyou

**SESSION 6C SIGNAL INTEGRITY AND
CLOCK DESIGN**

Moderators: Cheng-Kok Koh - Purdue Univ., West Lafayette, IN
Tong Gao - Monterey Design Systems, Inc., Sunnyvale, CA

This section deals with fundamental issues on signal integrity and clock design. The first paper addresses shielding for reduction of inductive noise. The second paper proposes a hybrid mesh/tree clock network structure. The third paper proposes a novel attempt to use the clock as shield for reduction of crosstalk.

**6C.1 FORMULAE AND APPLICATIONS OF INTERCONNECT ESTIMATION
CONSIDERING SHIELD INSERTION
AND NET ORDERING**

James Ma (dma@students.wisc.edu), Lei He - Univ. of Wisconsin, Madison, WI

6C.2 HYBRID STRUCTURED CLOCK NETWORK CONSTRUCTION

Haihua Su, Sachin S. Sapatnekar (sachin@ece.umn.edu) - Univ. of Minnesota, Minneapolis, MN

**6C.3 CASH: A NOVEL "CLOCK AS SHIELD" DESIGN METHODOLOGY FOR
NOISE IMMUNE PRECHARGE-EVALUATE LOGIC**

Yonghee Im (yonghee@ecn.purdue.edu) - Purdue Univ., West Lafayette, IN

Time: 2:00 PM to 3:30 PM

Room: Pine/Fir

SESSION 6D ANALOG SYNTHESIS

Moderators: Koen Lampaert - Mindspeed Tech., Newport Beach, CA
Henry Chang - Cadence Design Systems, Inc., San Jose, CA

Analog synthesis strives to automatically generate the design constraints, schematic sizing, and geometric layout of custom analog and RF circuits. The three papers in this session offer new techniques for automatic constraint recognition, simulation-based schematic sizing, and integrated sizing/layout for analog and RF designs.

**6D.1 THE SIZING RULES METHOD FOR ANALOG
INTEGRATED CIRCUIT DESIGN**

Helmut E. Graeb (graeb@ei.tum.de) - Technical Univ. of Munich, Munich, Germany
Stephan Zizala, Josef Eckmueller - Infineon Tech., Munich, Germany
Kurt Antreich - Technical Univ. of Munich, Munich, Germany

**6D.2 ASF: A PRACTICAL SIMULATION-BASED METHODOLOGY FOR THE
SYNTHESIS OF CUSTOM ANALOG CIRCUITS**

Michael J. Krasnicki (kraz@ti.com) - Texas Instruments Inc., Dallas, TX
Rodney Phelps - Carnegie Mellon Univ., Pittsburgh, PA
James R. Hellums, Mark McClung - Texas Instruments Inc., Dallas, TX
Rob A. Rutenbar, L. Richard Carley - Carnegie Mellon Univ., Pittsburgh, PA

**6D.3 A LAYOUT-AWARE SYNTHESIS METHODOLOGY
FOR RF CIRCUITS**

Peter J. Vancorenland, Geert Van der Plas (vdplas@esat.kuleuven.ac.be), Michiel Steyaert, Georges Gielen, Willy Sansen - Katholieke Univ., Leuven, Belgium

Tuesday, November 6, 2001

ICCAD-2001

Time: 4:00 PM to 5:30 PM

Room: Cedar

SESSION 7A MANUFACTURING TEST: STUCK-AT TO CROSSTALK

Moderators: Sujit Dey - Univ. of California at San Diego, La Jolla, CA
Yervant Zorian - LogicVision, Inc., San Jose, CA

Three structural testing topics are covered in this session, including a procedure to maximize the number of don't-cares in test patterns, a method for redundancy identification via efficient implication, and a current-based technique to detect crosstalk faults.

7A.1 ON IDENTIFYING DON'T CARE INPUTS OF TEST PATTERNS FOR COMBINATIONAL CIRCUITS

Seiji Kajihara (kajihara@cse.kyutech.ac.jp), Kohei Miyase - Kyushu Institute of Tech., Iizuka, Japan

7A.2 AN EFFICIENT FAULT ORIENTED PROCEDURE TO IDENTIFY REDUNDANT FAULTS IN COMBINATIONAL LOGIC CIRCUITS

Chen Wang (cwang@eng.uiowa.edu) - Univ. of Iowa, Iowa City, IA

Irith Pomeranz - Purdue Univ., West Lafayette, IN

Sudhakar M. Reddy - Univ. of Iowa, Iowa City, IA

7A.3 CROSSTALK FAULT DETECTION BY DYNAMIC IDD

Xiaoyun Sun (xsun@ece.umn.edu), Seonki Kim, Bapiraju Vinnakota - Univ. of Minnesota, Minneapolis, MN

SESSION 7B ARCHITECTURE ORIENTED SCHEDULING

Moderators: Miodrag Potkonjak - Univ. of California, Los Angeles, CA
Kazutoshi Wakabayashi - NEC Corp., Kawasaki, Japan

This session proposes novel synthesis techniques for specialized architectures. The first paper presents a new packing algorithm for different sized arrays. The second one targets specialized DSP compilers. The third one discusses the integrated formulation of scheduling.

7B.1 COLOR PERMUTATION: AN ITERATIVE ALGORITHM FOR MEMORY PACKING

Jianwen Zhu (jzhu@eecg.toronto.edu) - Univ. of Toronto, Toronto, ON, Canada

7B.2 CONSTRAINT SATISFACTION FOR RELATIVE LOCATION ASSIGNMENT AND SCHEDULING

Carlos A. Alba (alba@ics.ele.tue.nl) - Eindhoven Univ. of Tech., Eindhoven, The Netherlands

Bart Mesman - Philips Research Labs., Eindhoven, The Netherlands

Jochen Jess - Eindhoven Univ. of Tech., Eindhoven, The Netherlands

7B.3 A SUPER-SCHEDULER FOR EMBEDDED RECONFIGURABLE SYSTEMS

Seda Ogrenic Memik (seda@cs.ucla.edu) - Univ. of California, Los Angeles, CA

Time: 4:00 PM to 5:30 PM

Room: Pine/Fir

Time: 4:00 PM to 5:30 PM

Room: Donner/Siskiyou

SESSION 7C NEW TECHNIQUES IN ROUTING

Moderators: Jo Dale Carothers - Univ. of Arizona, Tucson, AZ
 Amir H. Farrahi - IBM Corp. TJ Watson Research Ctr.,
 Yorktown Heights, NY

This session addresses new techniques in the area of routing. The first paper presents a novel, multilevel framework for full-chip routing. The second paper proposes a multiple star net model, force-directed placement and maze searching technique. This session concludes with a paper that presents a new minimum-buffer routing formulation.

7C.1 MULTILEVEL APPROACH TO FULL-CHIP
 GRIDLESS ROUTING

Jason Cong, Jie Fang, Yan Zhang (zhangyan@cs.ucla.edu) -
 Univ. of California, Los Angeles, CA

7C.2 A FORCE-DIRECTED MAZE ROUTER

Fan Mo (fanmo@ic.eecs.berkeley.edu), Abdallah Tabbara,
 Robert K. Brayton - Univ. of California, Berkeley, CA

7C.3 MINIMUM-BUFFERED ROUTING OF NON-CRITICAL NETS FOR
 SLEW RATE AND RELIABILITY CONTROL

Charles J. Alpert - IBM Corp., Austin, TX
 Andrew B. Kahng, Bao Liu, Ion Mandoiu
 (mandoiu@cc.gatech.edu) - Univ. of California at San Diego,
 La Jolla, CA
 Alexander Zelikovskiy - Georgia State Univ., Atlanta, GA

Time: 4:00 PM to 5:30 PM

Room: Oak

SESSION 7D ISSUES IN SUBSTRATE COUPLING

Moderators: Mattan Kamon - Coventor, Inc., Cambridge, MA
 Kenneth L. Shepard - Columbia Univ., New York, NY

Substrate coupling is becoming very important in mixed signal design. In the first paper the authors utilize the singular value decomposition to generate a sparser representation of substrate coupling compared to wavelet based techniques. The second paper demonstrates the use of multilayer Green's functions and Gauss-Jacobi quadrature to speed-up inductance extraction in the presence of multilayered substrates. Finally, the third paper uses substrate coupling as an example of a strongly coupled interconnect system to present circuit simulation algorithms that must be employed to incorporate such systems in nonlinear circuit simulation.

7D.1 HIGHLY ACCURATE FAST METHODS FOR EXTRACTION AND
 SPARSIFICATION OF SUBSTRATE COUPLING BASED ON LOW-RANK
 APPROXIMATION

Joseph D. Kanapka (kanapka@mit.edu), Jacob K. White -
 Massachusetts Institute of Tech., Cambridge, MA

7D.2 FAST 3-D INDUCTANCE EXTRACTION IN
 LOSSY MULTI-LAYER SUBSTRATE

Minqing Liu (liumq@cse.ucsc.edu) - Univ. of California, Santa
 Cruz, CA
 Tiejun Yu - Cadence Design Systems, San Jose, CA
 Wayne W.-M. Dai - Univ. of California, Santa Cruz, CA

7D.3 SIMULATION APPROACHES FOR STRONGLY
 COUPLED INTERCONNECT SYSTEMS

Joel R. Phillips (jrp@cadence.com) - Cadence Design Systems,
 Inc., San Jose, CA
 Luis M. Silveira - Technical Univ. of Lisbon, Lisboa, Portugal

Time: 8:30 AM to 10:00 AM

Room: Cedar

SESSION 8A COMBINATIONAL OPTIMIZATION

Moderators: Olivier Coudert - Monterey Design Systems, Inc., Sunnyvale, CA
Tiziano Villa - Parades Labs., Rome, Italy

This section features advances in combinatorial and Boolean optimization, from classical two-level logic, to BDD minimization and applications, and finally to a general problem-solving frame for discrete optimization.

8A.1 BOOM - A HEURISTIC BOOLEAN MINIMIZER

Jan Hlavicka (hlavicka@fel.cvut.cz), Petr Fiser - Czech Tech. Univ., Prague 2, Czech Republic

8A.2 FASTER SAT AND SMALLER BDDS VIA COMMON FUNCTION STRUCTURE

Fadi A. Aloul (faloul@eecs.umich.edu), Igor L. Markov, Karem A. Sakallah - Univ. of Michigan, Ann Arbor, MI

8A.3 RECURSIVE BIPARTITIONING OF BDDS FOR PERFORMANCE DRIVEN SYNTHESIS OF PASS TRANSISTOR LOGIC CIRCUITS

Rupesh S. Shelar (rupesh@mail.ece.umn.edu), Sachin S. Sapatnekar - Univ. of Minnesota, Minneapolis, MN

8A.4 A PROBABILISTIC CONSTRUCTIVE APPROACH TO OPTIMIZATION PROBLEMS

Jennifer L. Wong (jwong@cs.ucla.edu) - Univ. of California, Los Angeles, CA
Farinaz Koushanfar - Univ. of California, Berkeley, CA
Seapahn Meguerdichian, Miodrag Potkonjak - Univ. of California, Los Angeles, CA

SESSION 8B REAL TIME SCHEDULING AND PERFORMANCE ANALYSIS

Moderators: Pai Chou - Univ. of California, Irvine, CA

Luciano Lavagno - Cadence Berkeley Labs., Berkeley, CA
Scheduling and performance analysis are fundamental challenges in real-time embedded system design. For applications where maximizing battery life is a major concern, tradeoffs must be made between energy consumption and satisfying timing constraints. The first paper of this session proposes a cost function to model the tradeoffs and a related optimization technique. The next two papers discuss approaches to estimating the timing performance of real-time systems. The second paper introduces an efficient technique to estimate the utilization bounds of real-time tasks with precedence constraints. The third paper extends a commercial discrete event simulator to facilitate the worst-case timing analysis.

8B.1 ENERGY EFFICIENT REAL-TIME SCHEDULING

Amit Sinha (sinha@mit.edu), Anantha P. Chandrakasan - Massachusetts Institute of Tech., Cambridge, MA

8B.2 EFFICIENT PERFORMANCE ESTIMATION FOR GENERAL REAL-TIME TASK SYSTEMS

Hongchao Liu (hliu@nd.edu), Xiaobo (Sharon) Hu - Univ. of Notre Dame, Notre Dame, IN

8B.3 STARS IN VCC: COMPLEMENTING SIMULATION WITH WORST-CASE ANALYSIS

Felice Balarin (felice@cadence.com) - Cadence Berkeley Labs., Berkeley, CA

Time: 8:30 AM to 10:00 AM

Room: Donner/Siskiyou

SESSION 8C POWER ANALYSIS

Moderators: Anirudh Devgan - IBM Corp., Austin, TX
Carlo Guardiani - PDF Solutions, San Jose, CA

This session includes three papers that address three areas of power analysis. The first paper describes an efficient technique for power grid analysis. A battery model and its application to energy management is presented in the second paper. The last paper describes a power-delay model for dynamic CMOS gates.

8C.1 MULTIGRID-LIKE TECHNIQUE FOR
POWER GRID ANALYSIS

Joseph N. Kozhaya - Univ. of Illinois Urbana, Urbana, IL
Sani R. Nassif - IBM Corp., Austin, TX
Farid N. Najm (f.najm@toronto.edu) - Univ. of Toronto,
Toronto, ON, Canada

8C.2 AN ANALYTICAL HIGH-LEVEL BATTERY MODEL
FOR USE IN ENERGY MANAGEMENT OF
PORTABLE ELECTRONIC SYSTEMS

Daler Rakhmatov (daler@ece.arizona.edu), Sarma Vrudhula -
Univ. of Arizona, Tucson, AZ

8C.3 POWER-DELAY MODELING OF DYNAMIC CMOS
GATES FOR CIRCUIT OPTIMIZATION

Jose L. Rossello (dfsjrs4@ps.uib.es), Jaime Segura - Balearic
Islands Univ., Palma de Mallorca, Spain

Time: 8:30 AM to 10:00 AM

Room: Oak

SESSION 8D TIMING AND NOISE ANALYSIS

Moderators: Tim Burks - Magma Design Automation, Inc.,
Cupertino, CA
Florentin Dartu - Intel Corp., Hillsboro, OR

This session contains three papers that address pressing problems in timing and noise analysis. The first addresses the problem of generating static timing models of custom transistor level circuits using symbolic timing simulation. The second paper describes a comprehensive evaluation of methods for computing transition times in static timing analysis. The third uses functional information to reduce the number of failures reported in noise analysis.

8D.1 A SYMBOLIC SIMULATION-BASED METHODOLOGY
FOR GENERATING BLACK-BOX TIMING MODELS
CUSTOM MACROCELLS

Clayton B. McDonald (clayton@ece.cmu.edu), Randal E.
Bryant - Carnegie Mellon Univ., Pittsburgh, PA

8D.2 ON THE SIGNAL BOUNDING PROBLEM
IN TIMING ANALYSIS

Jin-Fuw Lee (jinfuw@us.ibm.com), Daniel L. Ostapko, -
IBM Corp., Yorktown Heights, NY,
Jeffery Soreff - IBM Corp., Fishkill, NY
C.K. Wong - Chinese Univ. of Hong Kong, Shatin,
NT, Hong Kong

8D.3 FALSE-NOISE ANALYSIS USING LOGIC IMPLICATIONS

Alexey Glebov, Sergey Gavrilov, David T. Blaauw
(david.blaauw@motorola.com), Jingyan Zuo, Supamas
Sirichotiyakul, Chanhee Oh, Vladimir Zolotov - Motorola, Inc.,
Austin, TX

Time: 10:30 AM to 12:00 PM

Room: Cedar

SESSION 9A SYSTEM LEVEL TEST AND RELIABILITY

Moderators: Bapi Vinnakota - Univ. of Minnesota, Minneapolis, MN
Seiji Kajihara - Kyushu Institute of Tech., Iizuka, Japan

This session presents solutions for high-level test and reliability problems, including test application time and power reduction for system-on-chips, high-level fault modeling of bridging defects, and reliability through algorithm level re-computation.

9A.1 THE DESIGN AND OPTIMIZATION OF SOC TEST SOLUTIONS

Erik Larsson (erila@ida.liu.se), Zebo Peng - Linköping Univ., Linköping, Sweden
Gunnar Carlsson - Ericsson, Stockholm, Sweden

9A.2 ACCURATE CMOS BRIDGE FAULT MODELING WITH NEURAL NETWORK-BASED VHDL SABOTEURS

Don B. Shaw (shaw-d@rnc.ca) - Gennum Corp., Burlington, ON, Canada
Dhamin Al Khalili, Come N. Rozon - Royal Military College of Canada, Kingston, ON, Canada

9A.3 ALGORITHM LEVEL RE-COMPUTING: A REGISTER TRANSFER LEVEL CONCURRENT ERROR DETECTION TECHNIQUE

Kaijie Wu (kwu03@utopia.poly.edu), Ramesh Karri - Polytechnic Univ., Brooklyn, NY

Time: 10:30 AM to 12:00 PM

Room: Pine/Fir

SESSION 9B POWER ISSUES IN HIGH LEVEL SYNTHESIS

Moderators: Sridevan Parameswaran - The Univ. of New South Wales, Kensington, Australia
Nikil Dutt - Univ. of California, Irvine, CA

This session addresses power and energy issues in High-Level Synthesis. The first two papers present formulations dealing with transient power management and network-flow based integrated scheduling and binding. The third paper explores the limits of energy savings using dynamic voltage scaling.

9B.1 TRANSIENT POWER MANAGEMENT THROUGH HIGH LEVEL SYNTHESIS

Vijay Raghunathan (vijay@ee.ucla.edu) - Univ. of California, Los Angeles, CA
Sri Ravi, Anand Raghunathan, Ganesh Lakshminarayana - NEC Corp., Princeton, NJ

9B.2 AN INTEGRATED DATA PATH OPTIMIZATION FOR LOW POWER BASED ON NETWORK FLOW METHOD

Chungi Lyuh, Taewhan Kim (tkim@cs.kaist.ac.kr) - KAIST, Taejeon, Korea
C.L. Liu - National Tsing-Hua Univ., Hsinchu, Taiwan, ROC

9B.3 WHAT IS THE LIMIT OF ENERGY SAVING BY DYNAMIC VOLTAGE SCALING?

Gang Qu (gangqu@eng.umd.edu) - Univ. of Maryland, College Park, MD

Time: 10:30 AM to 12:30 PM

Room: Donner/Siskiyou

SESSION 9C ADVANCES IN PLACEMENT

Moderators: Jason Cong - Univ. of California, Los Angeles, CA
 Patrick Groeneveld - Magma Design Automation, Inc.,
 Cupertino, CA

This session includes three papers on advances in digital integrated circuit placement. The first paper presents a placement refinement technique based on local search. The next paper addresses post-placement congestion reduction. The final paper presents detailed placement for transistor-level layout.

- 9C.1 LOCAL SEARCH FOR FINAL PLACEMENT IN VLSI DESIGN
 Oluf Faroe, David Pisinger, Martin Zachariasen (martinz@diku.dk)
 - Univ. of Copenhagen, Copenhagen, Denmark
- 9C.2 CONGESTION REDUCTION DURING PLACEMENT WITH PROVABLY
 GOOD APPROXIMATION BOUND
 Xiaojian Yang (xjyang@cs.ucla.edu), Ryan Kastner, Majid
 Sarrafzadeh - Univ. of California, Los Angeles, CA
- 9C.3 DIRECT TRANSISTOR-LEVEL LAYOUT
 FOR DIGITAL BLOCKS
 Prakash Gopalakrishnan (prakashg@ece.cmu.edu), Rob A.
 Rutenbar - Carnegie Mellon Univ., Pittsburgh, PA

Time: 10:30 AM to 12:30 PM

Room: Oak

SESSION 9D INTERCONNECT ANALYSIS
 AND EXTRACTION

Moderators: Dennis M. Sylvester - Univ. of Michigan, Ann Arbor, MI
 Mustafa Celik - Monterey Design Systems, Inc.,
 Sunnyvale, CA

This session addresses recent advances in interconnect analysis techniques with particular regard to inductance issues. The first paper describes a new model order reduction approach that accounts for interconnect process variability. Next, a surface integral approach to inductance extraction is investigated. Finally, the third paper presents techniques useful in achieving efficient full-chip coupled RLC extraction.

- 9D.1 MODEL REDUCTION OF VARIABLE-GEOMETRY INTERCONNECTS
 USING VARIATIONAL SPECTRALLY-WEIGHTED BALANCED
 TRUNCATION
 Payam Heydari (payam@sahand.usc.edu) - Univ. of California,
 Irvine, CA
 Massoud Pedram - Univ. of Southern California,
 Los Angeles, CA
- 9D.2 IMPROVING THE ROBUSTNESS OF A SURFACE
 INTEGRAL FORMULATION FOR WIDEBAND
 IMPEDANCE EXTRACTION OF 3D STRUCTURES
 Zhenhai Zhu (zhzhu@rle-vlsi.mit.edu) - Massachusetts Institute of
 Tech., Cambridge, MA
 Jingfang Huang - Univ. of North Carolina, Chapel Hill, NC
 Jacob K. White, Ben Song - Massachusetts Institute of Tech.,
 Cambridge, MA
- 9D.3 PRACTICAL CONSIDERATIONS IN RLCK CROSSTALK ANALYSIS FOR
 DIGITAL INTEGRATED CIRCUITS
 Steven C. Chan (schan@cadence.com) - Cadence Design
 Systems, Inc., San Jose, CA
 Kenneth L. Shepard - Columbia Univ., New York, NY

Time: 2:00 PM to 3:30 PM

Room: Cedar

SESSION 10A DON'T CARE OPTIMIZATION AND BOOLEAN MATCHING

Moderators: Yuji Kukimoto - Silicon Perspective Corp., Santa Clara, CA
Prabhakar Kudva - IBM Corp. TJ Watson Research Ctr.,
Yorktown Heights, NY

This session presents theoretical and practical contributions in the optimization of multilevel logic networks. Two papers explore how to capture and exploit flexibility. One paper deals with the canonical for Boolean functions for Boolean matching in unate library.

- 10A.1 **SINGLE-PASS REDUNDANCY ADDITION AND REMOVAL**
Chih-Wei (Jim) Chang (cwchang@cornet.ece.ucsb.edu),
Malgorzata Marek-Sadowska - Univ. of California, Santa
Barbarba, CA
- 10A.2 **EFFICIENT CANONICAL FORM FOR BOOLEAN MATCHING OF
COMPLEX FUNCTIONS IN
LARGE LIBRARIES**
Jovanka Ciric (jovanka@synplicity.com) - Synplicity Inc.,
Sunnyvale, CA
Carl Sechen - Univ. of Washington, Seattle, WA
- 10A.3 **COMPATIBLE OBSERVABILITY DON'T CARES REVISITED**
Robert K. Brayton (brayton@eecs.berkeley.edu) - Univ. of
California, Berkeley, CA

Time: 2:00 PM to 3:30 PM

Room: Pine/Fir

SESSION 10B POWER SAVING TECHNIQUES FOR EMBEDDED PROCESSORS

Moderators: Preeti Panda - Synopsys, Inc., Mountain View, CA
Tony Givargis - Univ. of California, Irvine, CA

Several techniques are currently explored in order to allow the design of energy efficient embedded processors. The first paper introduces a methodology and tool-suite for the design of application specific instruction set processors. The methodology is illustrated with the design of a low power ASIP. The second and third paper discuss energy reduction techniques related to instruction placement and fetching. A compression technique based on dynamic reconfiguration to minimize bus activity is proposed in the second paper. The last paper proposes a new instruction code placement technique to minimize cache misses.

- 10B.1 **A METHODOLOGY FOR THE DESIGN OF APPLICATION SPECIFIC
INSTRUCTION SET PROCESSORS (ASIP) USING THE MACHINE
DESCRIPTION LANGUAGE LISA**
Andreas Hoffmann (hoffmann@ert.rwth-aachen.de), Oliver
Schliebusch, Achim Nohl, Gunner Braun, Oliver Wahlen, Heinrich
Meyr - Aachen Univ. of Tech., Aachen, Germany
- 10B.2 **AREA AND POWER REDUCTION OF EMBEDDED DSP SYSTEMS USING
INSTRUCTION COMPRESSION AND
RE-CONFIGURABLE ENCODING**
Subash Chandar Govindarajan (subba@india.ti.com) - Texas
Instruments India Ltd., Bangalore, India
Govindarajan Ramaswamy - Indian Institute of Science,
Bangalore, India
Mahesh Mehendale - Texas Instruments India Ltd., Bangalore, India
- 10B.3 **I-COPES: FAST INSTRUCTION CODE PLACEMENT FOR EMBEDDED
SYSTEMS TO IMPROVE PERFORMANCE AND ENERGY EFFICIENCY**
Sridevan Parameswaran - The Univ. of New South Wales,
Kensington, Australia
Joerg Henkel (henkel@ccrl.nj.nec.com) - NEC Corp., Princeton, NJ

Time: 2:00 PM to 3:30 PM

Room: Donner/Siskiyou

SESSION 10C EMBEDDED TUTORIAL:
IC POWER DISTRIBUTION CHALLENGES

Moderator: Farid Najm - Univ of Toronto, Toronto, ON, Canada

10C.1 DESIGN AND ANALYSIS OF POWER DISTRIBUTION NETWORKS
IN HIGH PERFORMANCE MICROPROCESSORS

Tyler Thorp (tylerthorp@yahoo.com), Kathir Aingaran,
Sudhakar Bobba - Sun Microsystems Inc., Sunnyvale, CA

This embedded tutorial will provide a summary of the power design challenges faced by high-performance IC designs. The talk will be broken into two parts. The first part will discuss power delivery issues such as EM, IR, ground bounce, modeling and design of the decap hierarchy, decap insertion and verification, and power grid trade-offs. The second part will discuss power management issues such as power estimation at various stages of a design cycle, power estimation at different levels of abstraction, and optimization of power management vs. performance.

10C.2 CHALLENGES IN POWER-GROUND INTEGRITY

Shen Lin (shen_lin@apache-da.com), Norman Chang - Apache Design Solutions, Inc., Palo Alto, CA

With the advance of semiconductor manufacturing, EDA, and VLSI design technologies, circuits with increasingly higher speed are being integrated at an increasingly higher density. This trend causes correspondingly larger voltage fluctuations in the on-chip power distribution network due to IR-drop, L di/dt noise, or LC resonance. Assuming constant field scaling, the percentage of di/dt to Vdd scales as S^4 when scaling process by $1/S$. Therefore, Power-Ground integrity becomes a serious challenge in designing future high-performance circuits. In this tutorial, we will introduce Power-Ground integrity, addressing its importance, verification methodology, and problem solution.

Wednesday, November 7, 2001

ICCAD-2001

SESSION 11A • WEDNESDAY NIGHT PANEL
AUTOMATIC HIERARCHICAL DESIGN:
FANTASY OR REALITY?

Time: 4:00 PM to 5:30 PM

Room: Pine/Fir

Moderator: Rob A. Rutenbar - Carnegie Mellon University,
Pittsburgh, PA

The debate regarding the design of integrated systems flat versus hierarchically is almost as old as VLSI design itself. Through the years experts have predicted that future generations of design automation tools would have to adopt a strictly hierarchical scheme for mastering algorithmic and logistic complexity. However, the steady improvement of tools and algorithms and the desire to push integrated circuit performance to the ultimate extremes has pushed the flat design style into the multi-million gate domain. Will this development continue, or will hierarchy finally win? The panel will discuss the different views on this topic and explore possible options for future design and tool flows. In particular, the panel will address questions related to verification, system design, logic synthesis, and physical design.

Panelists:

Olivier Coudert - Monterey Design Systems, Inc., Sunnyvale, CA
Patrick Groeneveld - Magma Design Automation, Cupertino, CA
Juergen Koehl - IBM Microelectronics, Essex Junction, VT
Scott Peterson - LSI Logic, Milpitas, CA
Vivek Raghavan - Avant!, Fremont, CA
Naresh Soni - STMicroelectronics, Inc., San Diego, CA

Tutorials9:00 AM - 5:00 PM

Registration8:00 AM - 10:00 AM

Tutorial 1 - Electrical-Integrity Design and Verification for Digital and Mixed-Signal Systems-On-A-Chip

Cedar Ballroom

Speakers: Dennis Sylvester - Univ. of Michigan, Ann Arbor, MI
Kenneth L. Shepard - Columbia Univ., New York, NY

Background: With rising clock rates and scaling technology, it is becoming increasingly necessary to design and model a very complex on chip electrical environment dominated by wires. In this tutorial, we describe the latest design and analysis approaches to ensuring the electrical integrity of today's systems-on-a-chip, tackling emerging problems such as inductance, substrate coupling, and power-supply integrity. This tutorial is designed for a target audience consisting of VLSI designers, managers, CAD tool developers, R&D engineers, and academic researchers. The goal is to enable attendees to address key interconnect-centric issues including all aspects of signal integrity, inductive effects, and high-performance clock and power distribution.

Description: We begin by describing the design and analysis techniques for signal integrity in deep submicron designs. We introduce the overall design flow and fundamental theories and concepts of RC/RLC interconnect analysis. We discuss the effects of capacitive and inductive coupling on line delay and noise. Design techniques to minimize capacitance and inductance effects are explored. We also focus on inductance estimation, extraction, and analysis.

The impact of environmental factors including variations in power supply voltage, temperature, and physical factors due to process variations also affect the cycle time and design robustness. Large die sizes and higher operating frequencies, coupled with large on-die variations at reduced device geometries, call for special consideration of this type of "noise".

We then consider power supply integrity analysis for systems-on-a-chip, including IR and Ldi/dt analysis with full consideration of decoupling capacitance, switching activity, and package models. Power distribution methodologies will be discussed. Substrate coupling is also becoming an important new design and analysis concern for mixed-signal designs. Substrate effects will be considered in the context of substrate noise analysis, latch-up and ESD analysis, and high-frequency interconnect analysis. In addition to analysis, we will also consider design techniques for limiting all of these coupling interactions.

We will survey various clock distribution approaches and the applicability for large SoC designs. We will compare approaches such as H-tree, mesh, grid for a typical design in terms of requirements including local/global skew, jitter, slew rates, power, buffer area, clock wiring resources, and shielding area. We will review the latest approaches for clock distribution networks including usage of de-skew units to reduce the clock skew.

Throughout the tutorial we will consider measurement techniques and structures for calibrating and characterizing the on-chip electrical environment with an emphasis on interconnect and substrate effects. This is important for technology characterization, yield analysis, and modeling validation.

Tutorials9:00 AM - 5:00 PM

Registration8:00 AM - 10:00 AM

**Tutorial 2 - Boolean Satisfiability Solving and its Application
in Equivalence and Model Checking**

Pine Ballroom

Speakers: Joao Marques-Silva - Tech. Univ. of Lisbon, Lisboa, Portugal
Per Bjesse - Prover Tech., Portland, OR
Wolfgang Kunz - Univ. of Frankfurt, Frankfurt, Germany

Background: This tutorial covers the most recent work in Boolean Satisfiability algorithms and its application in two key Design Automation applications: Equivalence Checking and Model Checking. The target audience consists of circuit designers interested in a better understanding of SAT technology, CAD engineers, and academic researchers working on SAT or on applications of SAT.

Description: The first section reviews the basic definitions for Boolean Satisfiability (SAT), surveys the more well-known applications of SAT in Electronic Design Automation (EDA), and introduces basic SAT algorithms and techniques.

The second section addresses state-of-the-art algorithms for SAT, covering the most well-known and used search techniques: non-chronological backtracking, clause recording, randomization, and restarts. Moreover, this section details the techniques recently proposed for fast implementation of SAT solvers. In addition, this section surveys recent research work in SAT, highlighting the techniques that show promise for the near future.

The third section focuses on algorithms and data structures for applying SAT in synthesis and combinational verification. In this application domain, SAT algorithms operate on CNF formulas representing circuits. This can be taken into account by specific heuristics. In this context we also discuss algorithms of automatic test pattern generation (ATPG) and compare them with related SAT algorithms.

The fourth section describes the application of SAT-algorithms in equivalence checking. We give an introduction to state-of-the-art equivalence checking algorithms, and focus on the role of SAT in equivalence checking.

The fifth section focuses on how SAT methods can be used to check properties of sequential circuits. We first demonstrate how to model synchronous gate-level circuits and safety properties. After this, we introduce a technique called bounded model checking. Given a circuit and a safety property, this analysis uses SAT algorithms to search for paths leading to a state where the safety property is violated.

Finally, in the sixth section, we continue our investigation of SAT-based model checking. A troublesome aspect of bounded model checking is that although it excels at finding failures, it is not a practical method for proving that a given system is safe. We therefore demonstrate how bounded model checking can be generalized to SAT-based induction---a complete proof method for safety properties. Finally, we conclude by discussing SAT-based reachability analysis.

Tutorials9:00 AM - 5:00 PM

Registration8:00 AM - 10:00 AM

Tutorial 3 - Optimization Strategies for Physical Synthesis and Timing Closure

Oak Ballroom

Speakers: Charles J. Alpert - IBM Corp., Austin, TX
Sachin S. Sapatnekar - Univ. of Minnesota, Minneapolis, MN
Salil Raje - Monterey Design Systems, Inc., Sunnyvale, CA

Background: This tutorial overviews various optimization techniques that can be utilized within a physical synthesis tool and/or achieve timing closure. The target audience consists of circuit designers who utilize these techniques, CAD engineers, and academic researchers. Familiarity with basic concepts in physical design is assumed.

Description: The first part of the tutorial discusses strategies for buffer insertion and wire sizing for a given net, focusing on the two stage methodology of first constructing a Steiner tree, then applying dynamic programming optimization. We show how to manage capacitance, polarity, and slew constraints while also performing blockage-aware routing. We also discuss different approaches to interconnect planning and physical resource allocation.

The second part describes optimizations that may be made at the gate and transistor levels. We will primarily focus on optimizations for transistor and gate sizing and local resynthesis. Additionally, issues related to transistor level optimization under dual threshold voltages will be addressed.

The third part is related to the consideration of signal integrity issues in design. One aspect relates to the design of supply networks to provide reliable voltage levels. We show the potential dangers that unreliable supply networks can have on timing closure and routability. A methodology to deal with the reliability of supply voltages in the design planning process will be put forward.

The fourth part will integrate all the techniques discussed into a physical synthesis methodology. Several placement techniques will be reviewed. Pros and cons of each in light of physical synthesis for design closure will be discussed. Factors that affect design closure include Congestion, Scan, Clocking, Power Topology; each will be addressed using a coherent flow that will achieve the right trade-offs.