ICCAD-2000 at a Glance

FULL-DAY TUTORIALS

Continental Breakfast - 8:00AM - 9:00AM (Gateway Foyer)
Tutorial Registration - 8:00AM - 10:00AM (Bayshore Foyer)
Lunch - 12:00PM - 1:00PM (Gateway Foyer)

THURSDAY, NOVEMBER 9

9:00 AM	TUTORIAL 1	5:00 PM

Modern Physical Design: Algorithm Technology and Methodology

(CEDAR BALLROOM)

9:00 AM	TUTORIAL 2	5:00 PM

Interconnect-Centric Design and Analysis for Electrical Integrity in Systems-on-a-Chip

(PINE BALLROOM)

9:00 AM	TUTORIAL 3	5:00 PM

Symbolic Model Checking: Principles and Advanced Techniques

(FIR BALLROOM)

9:00 AM	TUTORIAL 4	5:00 PM

Gain-Based Logic Synthesis

(OAK BALLROOM)

TUTORIAL 1

Modern Physical design: algorithm technology and methodology

Time: **9:00 AM to 5:00 PM** Room: **Cedar**

Speakers:
Andrew B. Kahng - Univ. of California, Los Angeles, CA
Majid Sarrafzadeh - Univ. of California, Los Angeles, CA
Stan Chow - AmmoCore Technology, Inc., San Jose, CA

Background: This tutorial covers "the latest word" in physical chip implementation methodology and PD algorithm technology, going into more "detail" than the previous edition of the tutorial. The target audience consists of system and circuit designers who would benefit from understanding tool capabilities in this arena, CAD engineers (both R&D and support), design project managers, and academic researchers. Familiarity with basic PD methodology is assumed.

Description: The first section reviews PD implications of the process technology and system design roadmaps. A generic chip planning and implementation methodology will help set context. A review of fundamental PD problem formulations and algorithms will concentrate on latest developments in RTL and gate-level partitioning, block and coarse placement, top-level interconnect planning and optimization, and cell-based place-and-route. We motivate needs for incremental optimization techniques, handling incomplete design data, and new tool interactions and concurrent optimizations.

The second section focuses on "upstream interactions", between traditional PD and floorplanning and logic synthesis. Approaches to achieving a convergent, predictable implementation flow will be reviewed. These center on alternate methodologies for prediction/predictability and estimation, e.g., budgeting-based planning, small blocks + wireplanning, layout-driven logic synthesis, constant-delay methodology, etc. Attention will be given to performance and signal integrity optimizations.

The third section focuses on interactions with parasitic estimation, delay calculation, timing/power/SI validations, and static timing/noise analyses and characterizations. We discuss requirements for tight analysis loops, reconciliation of data models, and speed/accuracy of delay and noise estimates.

The fourth section describes new links between traditional PD and polygon-level optimizations (layout enhancements for manufacturability, layout-on-the-fly or liquid layout, etc.). Such linkages are becoming dominant in high-end ASIC methodologies due to manufacturing yield and die cost considerations.

Last, we compare the half-dozen leading variants in convergent RTL-down methodology, and how they respectively make demands on PD. This taxonomy includes recent methodologies that exploit distributed or parallel computational platforms, or that creatively invoke commodity SP&R to achieve greater design productivity.

TUTORIAL 2

INTERCONNECT-CENTRIC DESIGN AND ANALYSIS FOR ELECTRICAL INTEGRITY IN SYSTEMS-ON-A-CHIP

Time: **9:00 AM to 5:00 PM** Room: **Pine**

Speakers:
Dennis Sylvester - Univ. of Michigan, Ann Arbor, MI
Kenneth Shepard - Columbia Univ., New York, NY
Sudhakar Muddu - Silicon Graphics Inc., Mountain View, CA

Background: With rising clock rates and scaling technology, it is becoming increasingly necessary to design and model a very complex on chip electrical environment dominated by wires. In this tutorial, we describe the latest design and analysis approaches to ensuring the electrical integrity of today's systems-on-a-chip, tackling emerging problems such as inductance, substrate coupling, and power-supply integrity. This tutorial is designed for a target audience consisting of VLSI designers, managers, CAD tool developers, R&D engineers, and academic researchers. The goal is to enable attendees to address key interconnect-centric issues including all aspects of signal integrity, inductive effects, and high-performance clock and power distribution.

Description: We begin by describing the design and analysis techniques for signal integrity in deep submicron designs. We introduce the overall design flow and fundamental theories and concepts of RC/RLC interconnect analysis. We discuss the effects of capacitive and inductive coupling on line delay and noise. Design techniques to minimize capacitance and inductance effects are explored. In terms of analysis, we describe interconnect macromodeling in a static noise analysis framework. We also focus on inductance estimation, extraction, and analysis.

The impact of environmental factors including variations in power supply voltage, temperature, and physical factors due to process variations also affect the cycle time and design robustness. Large die sizes and higher operating frequencies, coupled with large on-die variations at reduced device geometries, call for special consideration of this type of “noise”.

We then consider power supply integrity analysis for systems-on-a-chip, including IR and Ldi/dt analysis with full consideration of decoupling capacitance, switching activity, and package models. Power distribution methodologies will be discussed. Substrate coupling is also becoming an important new design and analysis concern for mixed-signal designs. Substrate effects will be considered in the context of substrate noise analysis, latch-up and ESD analysis, RF device modeling, and high-frequency interconnect analysis (current returns through the substrate). In additional to analysis, we will also consider design techniques for limiting all of these coupling interactions.

We will survey various clock distribution approaches and the applicability for large SoC designs. We will compare approaches such as H-tree, mesh, grid for a typical design in terms of requirements including local/global skew, jitter, slew rates, power, buffer area, clock wiring resources, and shielding area. We will review the latest approaches for clock distribution networks including usage of de-skew units to reduce the clock skew.

Throughout the tutorial we will consider measurement techniques and structures for calibrating and characterizing the on-chip electrical environment with an emphasis on interconnect and substrate effects. This is important for technology characterization, yield analysis, and modeling validation.

TUTORIAL 3

Symbolic Model Checking: Principles and Advanced Techniques

Time: **9:00 AM to 5:00 PM** Room: **Fir**

Speakers:

Kenneth L. McMillan - Cadence Berkeley, Labs., Berkeley, CA
Kavita Ravi - Cadence Design Systems, Inc., New Providence, NJ
Fabio Somenzi - Univ. of Colorado, Boulder, CO

Background: The increasing cost of verification has spurred interest in formal methods. Over the last few years equivalence checkers have become popular, and model checking has been successfully used in many projects. Formal methods can significantly increase productivity, but an understanding of their strengths and limitations is crucial for their effectiveness. This tutorial surveys the foundations of model checking, addresses modeling and performance issues, and presents recent algorithmic advances.

Description: The tutorial is divided in four parts. The first part quickly reviews formal verification techniques in general. It presents an overview of the various methods for sequential and combinational verification, with emphasis on sequential. The objective of this first part is to establish context and motivation. The second part is an introduction to model checking. It discusses the representation of hardware circuits for model checking, and the types of properties that are commonly verified with model checking. Safety and liveness properties are defined. Temporal logics are introduced as languages to specify properties. CTL, LTL, and CTL* are presented and contrasted. Automata as a specification formalism are also reviewed. The notions of similarity relation are discussed. The mu-calculus is then introduced as the “object-code” of the various specification mechanisms, and the model checking algorithms for CTL, LTL, and CTL* are formulated in terms of it. Implicit (symbolic) and explicit enumeration algorithms are discussed for model checking. Binary Decision Diagrams are reviewed. Their application to symbolic model checking is examined. The generation of witnesses and counter examples is discussed.The third part of the tutorial deals with abstraction (reduction) techniques—-both manual and automated. It introduces the notions of compositional verification, abstract interpretations, and Assume/Guarantee reasoning. Several types of reduction are illustrated, including data domain reductions and symmetry reductions.The application of these techniques benefits from the support of a proof assistant, which is discussed.The fourth part of the tutorial discusses approximation-based modelchecking, semi-exhaustive techniques, and efficient fix point computation, examining the issues that are related to the capacity limits of current model checkers. Specialized techniques for invariant checking, including the representation of environmental constraints are addressed. The combination of BDDs and CNF SAT solvers for efficient model checking is discussed.

TUTORIAL 4

Gain-based logic synthesis

Time: **9:00 AM to 5:00 PM** Room: **Oak**

Speakers:

Prabhakar Kudva - IBM T.J. Watson Research Ctr., Yorktown Heights, NY
David Kung - IBM T.J. Watson Research Ctr., Yorktown Heights, NY
Ruchir Puri - IBM T.J. Watson Research Ctr., Yorktown Heights, NY
Leon Stok - IBM T.J. Watson Research Ctr., Yorktown Heights, NY

Background: There exists a large gap between full-custom design and standard ASIC design. Gigahertz micro-processors have been announced while most ASIC parts run at maximum speeds of around 200 Mhz. However, a significant part of this gap can be closed by using the appropriate libraries and synthesis techniques. The same techniques that allow us to synthesize all control logic for gigahertz micro-processors, also helps the time consuming design closure of large complex ASICs. This is especially the case, when decisions early in the process are mistargeted due to the use of misleading wireload models. Delay models parameterized by gain allow predictable pre-placement synthesis without wire-load models and a more rapid evaluation of the effect of changes on the timing, thereby speeding up the combined synthesis and placement process.

Description: Delay models parameterized by gain significantly enhance the design and timing closure problems we are seeing in today’s complex standard cell design methodologies. To use these techniques most effectively the libraries, algorithms and methodology need to be adapted. We will address all three of these and tie them together in a coherent methodology that enhances the predictability of the timing closure process.

We will revisit the circuit basics of standard cells and the creation of static delay models with emphasis on the construction of gain-based delay models. Guidelines for designing practical libraries and their implications will be discussed as well as efficient algorithms for timing analysis, and area and load calculation.

Gain-based delay models open the opportunities to the construction of a different class of synthesis algorithms. Technology mapping in particular can benefit from the load-independence property of these models. Recent algorithms from the literature will be discussed. Buffering and fanout tree construction are other examples of algorithms that can be made much more predictable. Wire and gate sizing will be revisited and shown how they can be done in this environment.

Gain-based synthesis opens the opportunity to synthesize predictably without wire-load models. The actual sizing can be postponed until deep in the physical design phases, resulting in a more reliable timing information and better identification of timing critical regions. A methodology will be described that ties these together.

This tutorial is intended for designers to get an insight in circuits and libraries for which very efficient algorithms exist to synthesize them, for CAD-tool developers to understand state-of-the art algorithms for rapid design closure on large designs and for their managers to get an insight in the applicability of gain-based synthesis techniques to their specific design problems.