# Thursday, November 9, 2006



**Continental Breakfast** .....8:00 am - 9:00 am
**Registration**.....8:00 am - 3:00 pm

**Tutorials** .....9:00 am - 5:00 pm
**Lunch** .....12:30 pm - 1:30 pm

**Pine Ballroom** 9:00 am - 12:30 pm

## Tutorial 1 - Enabling Variability Aware Analysis

**Organizer: Emre Tuncer** - *Magma Design Automation, Inc., Santa Clara, CA*

**Speakers: Louis Liu** - *TSMC, Hsin-Chu, Taiwan*
**Stuart Taylor** - *ATI, Santa Clara, CA*
**Alessandra Nardi** - *Magma Design Automation, Inc., Santa Clara, CA*

**Description:** Statistical static timing analysis (SSTA) has been the focus of many academic papers in recent years. There has been a lot of emphasis on methods and techniques by which SSTA can be conducted with reasonable accuracy and within current limitations of design cycle and machine capabilities. There are other important components to installing and deploying SSTA in design community and illustrate its value. Without foundry support and guidance, it will not be possible to get meaningful and useful results. Among designers, a clear and concise use model has to be established: is slack distribution good enough? Or are there other places where statistical analysis and sensitivity information would be useful? EDA tool solution needs to make sure methods and techniques used in SSTA are practical, more importantly it is compatible with foundry data, addresses designers needs and fits in the design flow. This tutorial will focus on how SSTA fits in the whole design chain from foundry to designers, including challenges for tool development.

**Fir Ballroom** 9:00 am - 12:30 pm

## Tutorial 2 - DFM: Impact of Manufacturing Reality on Design

**Organizer: Chris Mack** - *Consultant, Scientist, Austin, TX*

**Speakers: Chris Mack** - *Consultant, Scientist, Austin, TX*
**David Z. Pan** - *Univ. of Texas, Austin, TX*
**Evanthia Papadopoulou** - *IBM Corp., Yorktown Heights, NY*

**Description:** Design for Manufacturability (DFM) has received considerable interest of late as it has become clear that an extension of past design-rule approaches to insuring manufacturability is no longer adequate. In fact, the design rule explosion at each new technology node threatens to dramatically increase the time and cost to complete complex designs and to endanger yield as well as time to market. DFM is a catch-all phrase that encompasses a wide range of techniques used to keep design rules manageable, design costs tolerable, and final yield acceptable. This tutorial will be broken into three parts:

**Part 1 - Introduction to Lithography *(Chris Mack)*** Covers the basics of resolution, the RET approaches to extend resolution, and how these approaches lead to fundamental nonlinearities in the imaging process. Since many of the DFM technologies in use or under development today become increasingly important as the lithographic imaging process becomes more non-linear, a basic understanding of lithographic science and technology is required for a comprehensive understanding of DFM.

**Part 2 - Random Defect and Critical Area Modeling *(Evanthia Papadopoulou)*** Covers the basics of random spot defects, random defect yield models, and basic computational methods for the extraction of critical area.

**Part 3 - A Bottom-up Walk of Physical Design for Manufacturability *(David Z. Pan)*** Covers DFM in a bottom-up manner, including motivations for physical design for manufacturability; design-oriented/variational lithography modeling and shape-based electrical characterization; process-variation aware OPC; RET/CMP, and redundant-via aware routing; variation tolerant clock design.

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## Oak Ballroom 9:00 am - 12:30 pm

### Tutorial 3 - Power and Thermal Challenges for 65 nm and Below

**Organizer:** **Kaustav Banerjee** - *Univ. of California, Santa Barbara, CA*

**Speakers:** **Kaustav Banerjee** - *Univ. of California, Santa Barbara, CA*
**Paul Coteus** - *IBM Corp., Yorktown Heights, NY*
**Vivek De** - *Intel Corp., Hillsboro, OR*

**Description:** Power dissipation and thermal issues constitute one of the biggest challenges in the design of all nanometer-scale high-performance ICs. Power consumed by the ICs is converted into heat, which in turn, can affect device characteristics including leakage currents. These electrothermal effects within the chip can have a profound impact on the design, analysis and packaging/cooling techniques. Hence, management of power and thermal issues as well as simultaneous consideration of electrical and thermal effects (electrothermal co-design) will be critical for sub-65 nm designs.

This tutorial will provide both fundamental and advanced understanding of the power and thermal problems by examining issues at the device, circuit and system level. The first part of the tutorial will discuss device scaling trends, leakage modeling and estimation, and parameter variations. It will also discuss various innovative techniques to reduce power. The second part of this tutorial will focus on micro and macro-scale electrothermal issues arising due to power dissipation at the device/interconnect and chip level, respectively. It will also examine the implications of these electrothermal effects for device/circuit/system level performance, power dissipation and reliability. The third part of the tutorial will focus on chip and system level thermal management issues including state-of-the-art packaging and cooling techniques and their implications for performance, cost and reliability. It will also review advanced measurement and simulation of chip thermal profiles as well as hot-spot management.

## Pine Ballroom 1:30 pm - 5:00 pm

### Tutorial 4 - Enhancing Yield at 45nm: DFM Solutions from Different Perspectives

**Organizer:** **Alfred Wong** - *Magma Design Automation, Inc., Santa Clara, CA*
**Speakers:** **Alfred Wong** - *Magma Design Automation, Inc., Santa Clara, CA*
**Sorin Dobre** - *Qualcomm, Inc., San Diego, CA*
**Lars Liebmann** - *IBM Corp., Fishkill, NY*

**Description:** Increasing integrated circuit variability dictates a change in the existing design-to-silicon flow in order to maintain profitability of the semiconductor industry. Any successful design-for-manufacturability (DFM) approach must grapple with both random defects and systematic effects introduced by advanced processing technologies including sub-wavelength lithography and chemical-mechanical polishing. This tutorial examines DFM issues and solutions from the viewpoints of different types of semiconductor organizations ? fabless, integrated device manufacturer (IDM), and electronic design automation (EDA) companies.

The dynamic nature of design and process information, especially during early stages of a technology node, poses nontrivial logistical DFM challenges in an IDM environment. There is no single fit-all approach. The optimal DFM solution is product-specific, depending on the type of design (such as microprocessor or ASIC). These different solutions also pose both risks and potentials for model-based OPC. For a fabless design house, DFM efforts drive new system-on-chip (SoC) flows. A practical DFM approach must justify the extra resource it draws. A key factor for return of investment consideration is the impact of DFM activities on time-to-market and time-to-volume. To enable both accurate analyses and high throughput required by DFM design flows, EDA software must account for the effects of the multitude of processing variabilities in a sensible yet computation-efficient manner. Intelligent use of manufacturing models is key. Common among all is the requirement of a consistent design-manufacturing interface that enables these various flows.

With speakers representing the various types of semiconductor organizations, this tutorial illuminates the DFM problem from different angles. Attendees would gain an appreciation of the challenges of DFM, an understanding of practical state-of-the-art solutions, and a glimpse into the future of DFM for integrated circuits.

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## Tutorial 5 - Transistor, Cell, and Interconnect Modeling: Basics to Advances

**Organizer: Noel Menezes** - *Intel Corp., Hillsboro, OR*

**Speakers: Sivakumar P. Mudanai** - *Intel Corp., Hillsboro, OR*
**Noel Menezes** - *Intel Corp., Hillsboro, OR*
**Lei He** - *Univ. of California, Los Angeles, CA*

**Description:** An understanding of recent transistor, cell, and interconnect models that address the primary physical phenomena impacting design at the 65nm technology node and beyond is essential for CAD engineers, developers, and researchers. In the transistor modeling space, a new standard has emerged with the acceptance of the surface potential-based MOS model, PSP, by the Compact Modeling Council. Surface potential-based models are more physical than previous threshold voltage based models and offer higher accuracy for digital, analog and RF applications. In addition, modern transistor models are required to cover new physical phenomena relevant to state-of-the-art process technologies, like quantum mechanical confinement, gate leakage, non-quasi static effects, strain Si, lateral doping gradient effects, etc., while fulfilling the conflicting requirement of sufficient accuracy and solution speed for practical circuit simulations. Similarly, current-source-based cell models (CSMs) capable of implicitly handling nonlinear input waveforms, active receiver and interconnect loads, cross-capacitance, multiple input switching effects, and supply variation are receiving increased attention with the adoption of CSM variants by major EDA vendors in their timing analysis and library characterization offerings. With the dominant role of interconnects in determining integrated circuit performance, an in-depth understanding of RC (and L) extraction is essential. Furthermore, with the emerging importance of variations induced by manufacturing processes, variational interconnect modeling and extraction techniques are an active research topic. This tutorial which covers modeling basics in addition to the most recent advances is intended for novices as well as experts from associated fields.

**Oak Ballroom** 1:30 pm - 5:00 pm

## Tutorial 6 - Advanced Routing Techniques for Nanometer IC Designs

**Organizer: Jason Cong** - *Univ. of California, Los Angeles, CA*

**Speakers: Jason Cong** - *Univ. of California, Los Angeles, CA*
**Tong Gao** - *Synopsys, Inc., Mountain View, CA*
**Rob A. Rutenbar** - *Carnegie Mellon Univ., Pittsburgh, PA*

**Description:** In this tutorial, we present the challenges and solutions of advanced IC routing in nanometer technologies. The tutorial has three parts. In the first part, we present the core algorithms used in most routing systems, including those for global and detailed routing (both grid-based and gridless), with the emphasis on the scalable routing paradigms. The second part of the tutorial addresses the challenges and available solutions to large-scale IC routing in nanometer designs, including highly scalable runtime, flexible support of complex design rules for nanometer designs, and the strong need for design-for-manufacture (DFM) capabilities. We shall describe some of the latest design rules and the associated optimization techniques, model-based design rule analysis for DFM optimization, and report the results by leading commercial routing tools in these areas. Finally, we shall survey the challenges and discuss some solutions on routing for analog and mixed-signal designs, which is an area of growing interest, given the increasing adoption of system-on-a-chip (SOC) integration.