

Monday, November 6, 2006

Registration - 7:00 am - 6:00 pm (Bayshore Foyer)

Speakers' Breakfast - 7:30 am (Monterey Room)

9:00 **Opening Session & Keynote Address: *An Industry in Transition: Opportunities and Challenges in Next-Generation Microprocessor Design*** • Phil Hester - Corporate Vice President and Chief Technology Officer, AMD, Austin, TX (Pine/Fir Ballroom)

10:00

Coffee Break sponsored by: **ALTERA**

	Donner Ballroom	Oak Ballroom	Pine/Fir Ballroom	Cedar Ballroom
10:30	SESSION 1A Parasitic Simulation and Modeling	SESSION 1B Post-Placement Optimization Techniques	SESSION 1C Variation Modeling	SESSION 1D Embedded Tutorial: From Dual to Multi to Many Core: Opportunities and Challenges for Supporting the New Exponential
12:00	12:00 - 1:30 Lunch Break (Siskiyou Ballroom)			
12:30				

12:00

12:30

	SESSION 2A	SESSION 2B	SESSION 2C	SESSION 2D
1:30	Embedded Tutorial: UML and SystemC for Industrial ESL Design - Basic Principles and Applications	Efficient Delay Test Generation	Power Grid Analysis and Design	Optimization Techniques for Different Target Technologies
3:30	Coffee Break			

3:30

	SESSION 3A	SESSION 3B	SESSION 3C	SESSION 3D
4:00	Placement and Floorplanning	Digital and RF Test and Reliability	Statistical Timing Analysis	Power and Performance Optimizations on System Level Design
6:00	Reception • 6:00 pm - 6:30 pm (Gateway Foyer)			

6:00

PANEL: CAD RESEARCH: PAY NOW OR PAY LATER

6:30 pm - 8:00 pm (Pine/Fir Ballroom)

ACM/SIGDA Dinner & Member Meeting - Invited Speaker: Mary A. Olsson, Research VP, Gartner, San Jose, CA 8:00 - 9:30 pm (Siskiyou Ballroom)

Tuesday, November 7, 2006

Technology Fair - 10:00 am - 6:00 pm (Gateway Foyer)

	Donner Ballroom	Oak Ballroom	Pine/Fir Ballroom	Designer's Perspectives Cedar Ballroom	
8:30	SESSION 4A	SESSION 4B	SESSION 4C	SESSION 4D	
	Analog Simulation and Verification	Self Adaptation and Physical Awareness in High-Level Synthesis	Advances in Performance Modeling for Interconnect and Memory	Embedded Tutorial: Design and CAD Challenges in 45nm CMOS and Beyond:	
10:00	Coffee Break				
	Donner Ballroom	Oak Ballroom	Pine/Fir Ballroom	Cedar Ballroom	Siskiyou Ballroom
10:30	SESSION 5A	SESSION 5B	SESSION 5C	SESSION 5D	SESSION 5E
	Analog Design Automation Techniques	Challenges on System Level Interconnection	Placement Optimization for Timing, Noise and Power	Timing and Power Analysis	Robustness and Reliability in Design
12:00					
12:30	12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)		A Discussion of Professional Ethics Organized & Supported by IEEE CEDA • 1:00 - 1:45 Sierra/Cascade Ballroom		
2:00	SESSION 6A	SESSION 6B	SESSION 6C	SESSION 6D	SESSION 6E
	Thermal and Variability Issues in Architectures	Embedded Tutorial: Automation in Mixed-Signal Design: Reality Check in	Global Routing	Emerging Topics in Signal Integrity and Reliability	Design to Enable Verification
4:00	Coffee Break				
	SESSION 7A	SESSION 7B	SESSION 7C	SESSION 7D	SESSION 7E
4:30	Fault-Tolerant Energy Minimization Techniques for Real-Time Embedded Systems	Emerging Issues in Contemporaneous System Level Design	Clock and Buffer Synthesis	Thermal Analysis for the Nano Scale	Mixed Signal Design Experiences
6:00					
6:30	ICCAD DESIGNER'S PERSPECTIVES RECEPTION Supported by IEEE CEDA 6:00 pm - 7:00 pm (Bayshore Foyer)				
	ICCAD DINNER • 7:00 pm - 8:30 pm (Sierra/Cascade Ballroom) Designer's Perspective Sessions are shaded grey.				

Wednesday, November 8, 2006

Registration - 7:00 am - 6:00 pm (Bayshore Foyer) Speakers' Breakfast - 7:30 am (Monterey Room)

	Donner Ballroom	Oak Ballroom	Pine/Fir Ballroom	NANO Day Cedar Ballroom
8:30	SESSION 8A Advances in Embedded System Design	SESSION 8B Architectural Design Techniques for High Performance and Robustness	SESSION 8C Manufacturability and Power in Layout	SESSION 8D Embedded Tutorial: Emerging Nanoelectronics: Prospects, State of the Art and Opportunities for CAD
10:00	Coffee Break			
10:30	SESSION 9A Technology Driven Layout Methodologies	SESSION 9B Novel FPGA Architectures, Techniques and Designs	SESSION 9C Specification and Architecture Challenges in High-Level Synthesis	SESSION 9D Defect Tolerance for Nanoscale Architectures
12:00	12:00 - 2:00 Lunch Break (Siskiyou Ballroom)			
12:30	Keynote: Innovation in Electronic Design Automation 1:00 - 1:45 Siskiyou Ballroom Leon Stok - Director of Electronic Design Automation, IBM Corp., Hopewell Junction, NY			
2:00	SESSION 10A Dynamic Power Management	SESSION 10B Advances in Model Checking	SESSION 10C Novel Interconnect Methodologies	SESSION 10D Embedded Tutorial: Integrating Nanoelectronics, Biotechnology and MEMS/NEMS
4:00	Coffee Break			
4:30	SESSION 11A Embedded Tutorial: Design Rule Mitigation	SESSION 11B Accelerating Verification	SESSION 11C Model Order Reduction and Parametric Analysis	SESSION 11D Design and Modeling of Molecular-Scale Systems
6:00	Closing Reception sponsored by: intel. • 6:00 pm - 6:30 pm Nano Sessions are shaded grey.			

Thursday, November 9, 2006

Registration8:00 am - 3:00 pm
Continental Breakfast .8:00 am - 9:00 am

Tutorials9:00 am - 5:00 pm
Lunch12:30 pm - 1:30 pm

Registration Fees **IEEE/ACM Member - \$395.00** **Non-Member - \$490.00** **Student - \$355.00**

MORNING TUTORIALS 9:00 am - 12:30 pm	AFTERNOON TUTORIALS 1:30 pm - 5:00 pm
<p>Tutorial 1 <i>Pine Ballroom</i></p> <p>Enabling Variability Aware Analysis Organizer: Emre Tuncer - <i>Magma Design Automation, Inc., Santa Clara, CA</i> Speakers: Louis Liu - <i>TSMC, Hsin-Chu, Taiwan</i> Stuart Taylor - <i>ATI, Santa Clara, CA</i> Alessandra Nardi - <i>Magma Design Automation, Inc., Santa Clara, CA</i></p>	<p>Tutorial 4 <i>Pine Ballroom</i></p> <p>Enhancing Yield at 45nm: DFM Solutions from Different Perspectives Organizer: Alfred Wong - <i>Magma Design Automation, Inc., Santa Clara, CA</i> Speakers: Sorin Dobre - <i>Qualcomm, Inc., San Diego, CA</i> Lars Liebmann - <i>IBM Corp., Fishkill, NY</i> Alfred Wong - <i>Magma Design Automation, Inc., Santa Clara, CA</i></p>
<p>Tutorial 2 <i>Fir Ballroom</i></p> <p>DFM: Impact of Manufacturing Reality on Design Organizer: Chris Mack - <i>Consultant/Scientist, Austin, TX</i> Speakers: Chris Mack - <i>Consultant/Scientist, Austin, TX</i> David Z. Pan - <i>Univ. of Texas, Austin, TX</i> Evanthia Papadopoulou - <i>IBM Corp., Yorktown Heights, NY</i></p>	<p>Tutorial 5 <i>Fir Ballroom</i></p> <p>Transistor, Cell, and Interconnect Modeling: Basics to Advances Organizer: Noel Menezes - <i>Intel Corp., Hillsboro, OR</i> Speakers: Sivakumar P. Mudanai - <i>Intel Corp., Hillsboro, TX</i> Noel Menezes - <i>Intel Corp., Hillsboro, OR</i> Lei He - <i>Univ. of California, Los Angeles, CA</i></p>
<p>Tutorial 3 <i>Oak Ballroom</i></p> <p>Power and Thermal Challenges for 65 nm and Below Organizer: Kaustav Banerjee - <i>Univ. of California, Santa Barbara, CA</i> Speakers: Paul Coteus - <i>IBM Corp., Yorktown Heights, NY</i> Vivek De - <i>Intel Corp., Hillsboro, OR</i> Kaustav Banerjee - <i>Univ. of California, Santa Barbara, CA</i></p>	<p>Tutorial 6 <i>Oak Ballroom</i></p> <p>Advanced Routing Techniques for Nanometer IC Designs Organizer: Jason Cong - <i>Univ. of California, Los Angeles, CA</i> Speakers: Jason Cong - <i>Univ. of California, Los Angeles, CA</i> Tong Gao - <i>Synopsys, Inc., Mountain View, CA</i> Rob A. Rutenbar - <i>Carnegie Mellon Univ., Pittsburgh, PA</i></p>