

Continental Breakfast8:00 am - 9:00 am
Registration.....8:00 am - 3:00 pm

Tutorials9:00 am - 5:00 pm
Lunch12:00 pm - 1:30 pm

For 2005, ICCAD has five exciting tutorials presented by recognized domain experts and dealing with current and emerging hot topics. Two tutorials focus on the important area of variability; the first of these tutorials recognizes the need for a new generation of gate modeling tools and techniques to enable accurate and consistent manufacturing-aware timing analysis, while the second tutorial focuses on yield maximization algorithms that can leverage statistical timing analysis to improve design manufacturability. Two other tutorials are in the analysis area, one in the emerging and important discipline of package-chip co-design, and the other on the re-emergence of circuit simulation as a central requirement for dealing with the numerous issues being faced in nm-scale designs (presented by the author of the original Spice). Last, but by no means least, is a tutorial on C-based design, showing how this crucial next step in design abstraction is going to enable a new generation of complex systems-on-chip designs.

Pine Ballroom 9:00 am - 12:30 pm

Tutorial 1 - Characterization and Gate Modeling for 90nm and Below

Organizer: Anirudh Devgan - *Magma Design Automation, Inc., Austin, TX*

Speakers: Dennis Sylvester - *Univ. of Michigan, Ann Arbor, MI*
Shakir Abbas - *Magma Design Automation, Inc., Santa Clara, CA*

Noel Menezes - *Intel Corp., Hillsboro, OR*

Description: With deep submicron designs well underway, the impact on characterizing and generating accurate models has been significant. What used to be a straightforward process has now become a much more data intensive and complex task due to increasing requirements on modeling features. For accurate deep submicron design sign-off, analysis tools now demand that models take into account signal integrity effects, more sophisticated driver and receiver models, advanced low power analysis using transient current waveforms and de-coupling capacitance, manufacturability and yield effects, as well as all the other traditional measurements. The characterization solutions need to find innovative ways to reduce the size of the models while maintaining a quick turn around time for characterizing a complete library to satisfy the requirements of designs at 90nm and below. This tutorial will present techniques for sub-90nm characterization and gate modeling and will present future challenges.

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Fir Ballroom

9:00 am - 12:30 pm

Oak Ballroom

9:00 am - 5:00 pm

Tutorial 2 - Package-Chip Co-Design

Organizer: Lei He - *Univ. of California, Los Angeles, CA*

Speakers: Anirudh Devgan - *Magma Design Automation, Inc., Austin, TX*

Shauki Elassaad - *Rio Design Automation, Santa Clara, CA*

Description: Larger number of IO cells, higher frequencies, tighter noise margins, and shorter time to market necessitate co-design of chip IO and package. In this tutorial, we will shed light on a new chip-package co-design paradigm and all the technologies necessary to enable it. The first part of the tutorial will present modeling and analysis techniques. Package modeling and extraction is a difficult problem given the large number of planes and millions of shapes that have to be modeled for capacitive, inductive and resistive effects. The tutorial will present techniques for efficient extraction using L-1 based modeling, distributed equivalent capacitance modeling and parallel processing. This part of the tutorial will also present analysis techniques for power grid and signal integrity verification. The second part of the tutorial will describe a chip-package co-design flow which supports packages with multiple dies hosting multiple GHz interfaces and multiple voltage domains. This type of design necessitates a holistic approach to the design of electronic systems that marries detailed modeling and abstraction of the various layers of chip-package co-design. We will describe the challenges and issues associated with the design of such systems with emphasis on package aware chip IO planning, package escape analysis and routing, timing, and signal and power integrity optimization.

Morning Tutorial

Tutorial 3 - ESL Design: Why the Time is Right and What are the Key Enabling Technologies

Organizer: Marcello Lajolo - *NEC Labs America, Princeton, NJ*

Speakers: Wolfgang Mueller - *Paderborn Univ., Paderborn, Germany*

Marcello Lajolo - *NEC Labs America, Princeton, NJ*

Marcello Coppola - *ST Microelectronics, Grenoble, France*

Felice Balarin - *Cadence Berkeley Labs., Berkeley, CA*

Luca P. Carloni - *Columbia Univ., New York, NY*

Tony Givargis - *Univ. of California, Irvine, CA*

Aarti Gupta - *NEC Labs America, Princeton, NJ*

Description: Although Moore's Law, in principle, enables a huge number of components to be integrated into a single chip, design methods that will allow system architects to put the component together to achieve cost, power and time-to-market targets are severely lacking. ESL design is quite compelling because it deals well with complexity by facilitating the creation of behavioral IP cores that are more re-usable than RTL IPs and also more suitable for HW/SW codesign. In this tutorial we cover ESL design fundamentals, motivation for ESL design, industry need and why the time is right for ESL design. We present support technologies (UML, behavioral synthesis, ASIPs, on-chip communication architectures, interface synthesis, and software for embedded systems) that are necessary for realizing the full potentials of ESL design. We also consider both simulation and verification aspects. For simulation, we address a problem of co-simulation of modules that are not only written in different languages, but also model the design at different levels of abstraction. For verification, we present recent developments in applying model checking techniques to C programs.

Full Day Tutorial

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Pine Ballroom 1:30 pm - 5:00 pm

Fir Ballroom 1:30 pm - 5:00 pm

Tutorial 4 - Simulation Technologies and Tools for the Nano Era

Organizer: Jaijeet Roychoudhury - Univ. of Minnesota, Minneapolis, MN

Speakers: Laurence W. Nagel - Omega Enterprises, Randolph, NJ
Yuri Sirenko - Berkeley Design Automation, Inc., Santa Clara, CA
Amit Narayan - Berkeley Design Automation, Inc., Santa Clara, CA

Description: After its heyday in the 1970s, circuit simulation - the first electronic CAD discipline and, arguably, the progenitor of the EDA industry - was largely eclipsed during the 80s and 90s by other areas of EDA such as physical and logic-level CAD. However, the past decade has seen a tremendous resurgence of interest and progress in simulation-related research and development. In this tutorial, we will provide a detailed overview of these developments and illustrate their value in enabling and sustaining increasingly complex design flows. Starting from a review of the history and fundamentals of analog simulation, we will outline developments in design that resulted in challenges to traditional simulation tools. We will then describe two topical areas where new simulation methods have made significant strides in addressing these challenges: fast hierarchical simulation and RF/mixed-signal algorithms. Our tutorial will balance coverage of algorithmic principles with illustrations of use in real design flows, employing cutting-edge examples from industry.

Tutorial 5 - Yield Maximization Algorithms

Organizer: Helmut Graeb - Technische Universitaet Muenchen, Munich, Germany

Speakers: Peter Feldmann - IBM TJ Watson Research Ctr., Yorktown Heights, NY
Helmut Graeb - Technische Universitaet Muenchen, Munich, Germany
Ulf Schlichtmann - Technische Universitaet Muenchen, Munich, Germany

Description: Increasing variability in deep submicron technologies has become a critical issue in modern digital circuit design. Classic process corner cases are no longer adequate to capture the worst-case delay behavior of critical paths with sufficient accuracy. We urgently need a shift to a statistical analysis and optimization of the timing behavior on gate and higher level. This tutorial presents the state-of-art in statistical timing analysis. As a similar shift in design philosophy from worst-case simulation to a true statistical design has already been done in the domain of analog circuits, we will first review statistical techniques for analog yield optimization and design centering. From that, we will move to statistical timing analysis of digital blocks and paths. In particular, we will look how the propagation of a delay distribution through a circuit can be computed, properly considering correlations due to reconvergent paths as well as process variations. We will also discuss requirements on the characterization and extraction of statistical data and look on future issues like parametric manufacturing test for digital circuits.