Tutorials ....9:00 AM - 5:00 PM Registration ....8:00 AM - 10:00 AM

Tutorial 1 - Electrical-Integrity Design and Verification for Digital and Mixed-Signal Systems-On-A-Chip

Cedar Ballroom

Speakers: Dennis Sylvester - Univ. of Michigan, Ann Arbor, MI
Kenneth L. Shepard - Columbia Univ., New York, NY

Background: With rising clock rates and scaling technology, it is becoming increasingly necessary to design and model a very complex on chip electrical environment dominated by wires. In this tutorial, we describe the latest design and analysis approaches to ensuring the electrical integrity of today's systems-on-a-chip, tackling emerging problems such as inductance, substrate coupling, and power-supply integrity. This tutorial is designed for a target audience consisting of VLSI designers, managers, CAD tool developers, R&D engineers, and academic researchers. The goal is to enable attendees to address key interconnect-centric issues including all aspects of signal integrity, inductive effects, and high-performance clock and power distribution.

Description: We begin by describing the design and analysis techniques for signal integrity in deep submicron designs. We introduce the overall design flow and fundamental theories and concepts of RC/RLC interconnect analysis. We discuss the effects of capacitive and inductive coupling on line delay and noise. Design techniques to minimize capacitance and inductance effects are explored. We also focus on inductance estimation, extraction, and analysis.

The impact of environmental factors including variations in power supply voltage, temperature, and physical factors due to process variations also affect the cycle time and design robustness. Large die sizes and higher operating frequencies, coupled with large on-die variations at reduced device geometries, call for special consideration of this type of "noise".

We then consider power supply integrity analysis for systems-on-a-chip, including IR and Ldi/dt analysis with full consideration of decoupling capacitance, switching activity, and package models. Power distribution methodologies will be discussed. Substrate coupling is also becoming an important new design and analysis concern for mixed-signal designs. Substrate effects will be considered in the context of substrate noise analysis, latch-up and ESD analysis, and high-frequency interconnect analysis. In addition to analysis, we will also consider design techniques for limiting all of these coupling interactions.

We will survey various clock distribution approaches and the applicability for large SoC designs. We will compare approaches such as H-tree, mesh, grid for a typical design in terms of requirements including local/global skew, jitter, slew rates, power, buffer area, clock wiring resources, and shielding area. We will review the latest approaches for clock distribution networks including usage of de-skew units to reduce the clock skew.

Throughout the tutorial we will consider measurement techniques and structures for calibrating and characterizing the on-chip electrical environment with an emphasis on interconnect and substrate effects. This is important for technology characterization, yield analysis, and modeling validation.

Thursday, November 8, 2001

Tutorials ....9:00 AM - 5:00 PM   Registration ....8:00 AM - 10:00 AM

Tutorial 2 - Boolean Satisfiability Solving and its Application in Equivalence and Model Checking

Pine Ballroom

Speakers: Joao Marques-Silva - Tech. Univ. of Lisbon, Lisboa, Portugal
Per Bjesse - Prover Tech., Portland, OR
Wolfgang Kunz - Univ. of Frankfurt, Frankfurt, Germany

Background: This tutorial covers the most recent work in Boolean Satisfiability algorithms and its application in two key Design Automation applications: Equivalence Checking and Model Checking. The target audience consists of circuit designers interested in a better understanding of SAT technology, CAD engineers, and academic researchers working on SAT or on applications of SAT.

Description: The first section reviews the basic definitions for Boolean Satisfiability (SAT), surveys the more well-known applications of SAT in Electronic Design Automation (EDA), and introduces basic SAT algorithms and techniques.

The second section addresses state-of-the-art algorithms for SAT, covering the most well-known and used search techniques: non-chronological backtracking, clause recording, randomization, and restarts. Moreover, this section details the techniques recently proposed for fast implementation of SAT solvers. In addition, this section surveys recent research work in SAT, highlighting the techniques that show promise for the near future.

The third section focuses on algorithms and data structures for applying SAT in synthesis and combinational verification. In this application domain, SAT algorithms operate on CNF formulas representing circuits. This can be taken into account by specific heuristics. In this context we also discuss algorithms of automatic test pattern generation (ATPG) and compare them with related SAT algorithms.

The fourth section describes the application of SAT-algorithms in equivalence checking. We give an introduction to state-of-the-art equivalence checking algorithms, and focus on the role of SAT in equivalence checking.

The fifth section focuses on how SAT methods can be used to check properties of sequential circuits. We first demonstrate how to model synchronous gate-level circuits and safety properties. After this, we introduce a technique called bounded model checking. Given a circuit and a safety property, this analysis uses SAT algorithms to search for paths leading to a state where the safety property is violated.

Finally, in the sixth section, we continue our investigation of SAT-based model checking. A troublesome aspect of bounded model checking is that although it excels at finding failures, it is not a practical method for proving that a given system is safe. We therefore demonstrate how bounded model checking can be generalized to SAT-based induction---a complete proof method for safety properties. Finally, we conclude by discussing SAT-based reachability analysis.

Tutorials ....9:00 AM - 5:00 PM   Registration ....8:00 AM - 10:00 AM

Tutorial 3 - Optimization Strategies for Physical Synthesis and Timing Closure

Oak Ballroom

Speakers: Charles J. Alpert - IBM Corp., Austin, TX
Sachin S. Sapatnekar - Univ. of Minnesota, Minneapolis, MN
Salil Raje - Monterey Design Systems, Inc., Sunnyvale, CA

Background: This tutorial overviews various optimization techniques that can be utilized within a physical synthesis tool and/or achieve timing closure. The target audience consists of circuit designers who utilize these techniques, CAD engineers, and academic researchers. Familiarity with basic concepts in physical design is assumed.

Description: The first part of the tutorial discusses strategies for buffer insertion and wire sizing for a given net, focusing on the two stage methodology of first constructing a Steiner tree, then applying dynamic programming optimization. We show how to manage capacitance, polarity, and slew constraints while also performing blockage-aware routing. We also discuss different approaches to interconnect planning and physical resource allocation.

The second part describes optimizations that may be made at the gate and transistor levels. We will primarily focus on optimizations for transistor and gate sizing and local resynthesis. Additionally, issues related to transistor level optimization under dual threshold voltages will be addressed.

The third part is related to the consideration of signal integrity issues in design. One aspect relates to the design of supply networks to provide reliable voltage levels. We show the potential dangers that unreliable supply networks can have on timing closure and routability. A methodology to deal with the reliability of supply voltages in the design planning process will be put forward.

The fourth part will integrate all the techniques discussed into a physical synthesis methodology. Several placement techniques will be reviewed. Pros and cons of each in light of physical synthesis for design closure will be discussed. Factors that affect design closure include Congestion, Scan, Clocking, Power Topology; each will be addressed using a coherent flow that will achieve the right trade-offs.