

**IEEE/ACM Workshop on Variability Modeling and Characterization**  
(<http://www.eas.asu.edu/~ycao/cvm>)

November 5<sup>th</sup> 2009, San Jose, CA, U.S.A.

Collocated with ICCAD 2009

Registration at <http://www.iccad.com/2009/index.html>

Workshop organizers: Yu Cao (Arizona State University)  
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It is widely recognized that process variation is emerging as a fundamental challenge to IC design in scaled CMOS technology; and it will have profound impact on nearly all aspects of circuit performance. While some of the negative effects of variability can be handled with improvements in the manufacturing process, the industry is starting to accept the fact that some of the effects are better mitigated during the design process. Handling variability in the design process will require accurate and appropriate models of variability and its dependence on designable parameters (i.e. layout), and its spatial and temporal distributions. It also requires carefully designed test structures and proper statistical data analysis methods to extract meaningful models from large volumes of silicon measurements. The resulting compact modeling of systematic, random, spatial, and temporal variations is essential to abstract the physical level variations into a format the designers (and more importantly, the tools they use) can utilize. This workshop provides a forum to discuss current practice as well as near future research needs in test structure design, variability characterization, compact variability modeling, and statistical simulation.

Key topics of this workshop includes (but not limited to):

- Physics mechanisms and technology trends of device-level variations.
- First-principles simulation methods for predicting variability.
- Time-dependent variation and their interaction with other variation sources
- Compact modeling of variations in transistors and interconnect.
- Device and circuit level modeling techniques.
- Test structure design for variability.
- Variability characterization and bounding.
- Statistical data analysis and model extraction methods.
- Novel implementation and simulation techniques for dealing with variability.

## **Tentative Program**

8:20 – 8:30am      **Opening Remarks**

8:30 – 10:00am      **Atomistic-Level Variations**

**Scott Roy** (Univ. of Glasgow): *Atomistic Simulation of Variability*

**Tsu-Jae King Liu** (Univ. of California, Berkeley): *Nanoscale Transistor Design  
Optimization in Consideration of Atomistic Effects*

**Naoki Tega** (Hitachi America): *Study on Variability in Transistor Characteristics due to  
Random Telegraph Noise*

10:00 – 10:30am      **Morning Break**

10:30 – 12:00pm      **Process Induced Variations**

**Paul Newman** (Intel): *Topology Matters: When a Sensitive Circuit Meets Transistor  
Variation*

**Puneet Gupta** (Univ. of California, Los Angeles): *Revisiting Variation Models and Their  
Reliability*

**Victor Moroz** (Synopsys): *Modeling Layout-Induced Proximity Effects*

12:00 – 1:30pm      **Lunch Break**

1:30 – 3:00pm      **Emerging Parametric Variations and Extraction**

**Tanya Nigam** (Global Foundries): *Challenges of Predicting Product Level Degradation  
from Simple Device Level Models*

**Abe Elfadel** (IBM): *Efficient Techniques for Variation-Aware Electrical Modeling and  
Verification of VLSI Interconnect*

**Xin Li** (Carnegie Mellon Univ.): *Virtual Probe: Minimum-Cost Silicon Characterization  
of Nanoscale Integrated Circuits*

3:00 – 3:30pm      **Afternoon Break**

3:30 – 5:00pm      **Characterization of Device and Circuit Variability**

**Vikas Chandra** (ARM): *Challenges of Designing Robust Physical IP in Nanoscale  
CMOS Technologies*

**Lawrence Clark** (Arizona State Univ.): *In-Situ Characterization of SRAM Variability*

**Chris Kim** (Univ. of Minnesota): *On-Chip Reliability Monitors: Circuit Ideas,  
Measurements and Limitations*

5:00 – 5:10pm      **Closing Remarks**