

Tutorial Registration Fees Apply

Please refer to page 44.

ICCAD is offering one full-day tutorial and four half-day tutorials. Registrants will receive the tutorial notes to all sessions. Attendees can pick and choose which morning and afternoon tutorials to attend. Registration includes access to all tutorials, hard copy notes to all sessions and morning and afternoon coffee breaks.

Donner Ballroom

8:30am - 5:30pm

Siskiyou Ballroom

8:30am - 12:30pm

Tutorial 1 - Refactoring to Concurrency

Organizer: Ken Wadland - Cadence Design Systems, Inc.,
Chelmsford, MA

Speakers: Ken Wadland - Cadence Design Systems, Inc.,
Chelmsford, MA

Rahul Agarwal - Cadence Design Systems, Inc.,
Berkeley, CA

Description: Server farms are already widely available and multi-core desktop systems are becoming increasingly common, yet most EDA software runs on only one CPU. One of the main causes for this gap is the difficulty of developing and debugging concurrent algorithms. In this full-day tutorial, participants will have hands-on experience converting a single-threaded application into one that is both multi-threaded and distributed. The conversion will be performed in a sequence of well-defined, discrete steps (called "refactorings"). Focus will be on protocols and techniques for debugging and testing.

Each concurrency topic will be introduced in lecture format using PowerPoint and live demonstrations. Each of these presentations will be followed by hands-on programming exercises and round-table discussions. All examples and exercises will be C++. Participants will need to bring their own Linux or Windows laptop to complete the exercises.

Tutorial 2 - Within-Die Variations in Timing: From Derating to CPPR to Statistical Methods

Organizer: Chandu Visweswariah - IBM Thomas J. Watson Research Center, Yorktown Heights, NY

Speaker: Chandu Visweswariah - IBM Thomas J. Watson Research Center, Yorktown Heights, NY

Description: Within-die variations throw a wicked curve ball at the classical static timing algorithm. This tutorial is a gentle-paced explanation of techniques used to handle these variations during timing. Within-die variations have traditionally been handled by an early/late split, bounding gate and wire delays between earliest and latest values by derating factors. Various other uncertainties and unknowns can be swept under the magic carpet of this early/late split. The first part of the tutorial will frame the problem and describe typical modeling methods.

Early/late splits cannot be accurately handled by block-based timing. A Common-Path Pessimism Removal (CPPR) step is required to recover unnecessary pessimism. A polynomial-time CPPR algorithm and several speedup "tricks" will be described in the second part.

Die-to-die variations can also be handled by extensions of CPPR called generalized CPPR, and several speedup methods are available. This will be covered in the third part.

Path-based methods such as CPPR are non-incremental and superlinear in complexity. To return to the simplicity, incrementality and linear-time behavior of block-based timing, statistical methods can be leveraged. These methods, which will be described in the fourth part, can be employed to achieve pessimism reduction, and efficient and incremental timing analysis. Methodology and optimization implications will be covered.

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*Cascade Ballroom**8:30am - 12:30pm**Siskiyou Ballroom**1:30pm - 5:30pm***Tutorial 3 - Addressing Variations – During Layout, Post-Layout and Post-Silicon****Organizer:** Praveen Elakkumanan - IBM Corp., Fishkill, NY

Speakers: Praveen Elakkumanan - IBM Corp., Fishkill, NY
 Raj Varada - Intel Corp., Santa Clara, CA
 James Culp - IBM Corp., Fishkill, NY
 Michael Orshansky - Univ. of Texas, Austin, TX

Description: This tutorial will discuss in detail the variability and consequent manufacturing challenges in nanoscale VLSI by taking a holistic approach in analyzing and addressing different effects. We classify and categorize the process variations into three different groups based on several characteristics - well understood systematic variations, variations with known "trend dependence" and completely random variations. We then present different flavors of the 3M concept - measure, model and mitigate to deal with all the above types of process variations. Specifically, this tutorial is divided into four parts and will discuss DFM/MFD technologies and methodologies that provide high-ROI bridges between the design and process communities to deal with the variability challenges:

Parts 1 & 2 interactions between layout and manufacturability, and their impact on circuit design (electrical behavior); DFM Vs MILD (Manufacturing Induced Layout Design); manufacturing aware timing closure; and Part 3 will go over some of the many accepted and possible mitigation techniques in design post processing (after tape-out). Finally, Part 4 will discuss analysis and optimization strategies for design in the presence of random variability; methods for post-silicon adaptivity via body biasing and supply voltage biasing, and about strategies for co-optimization between statistical design and post-silicon tuning.

Tutorial 4 - DFM Routing and Clock Distribution

Organizers: David Z. Pan - Univ. of Texas, Austin, TX
 Stefan Rusu - Intel Corp., Santa Clara, CA

Speakers: David Z. Pan - Univ. of Texas, Austin, TX
 Eric Nequist - Cadence Design Systems, Inc., San Jose, CA
 Simon Tam - Intel Corp., Santa Clara, CA

Description: Manufacturability and variability pose tremendous challenges in nanometer designs, due to manufacturing processes such as lithography and CMP, the inevitability of random defects, and environmental effects such as temperature and voltage variations. The resulting yield loss strongly depends on layout patterns. Routing and clock distribution are two key stages where layout embedding is performed, and they play a critical role in enhancing manufacturability and mitigating variation effects. The conventional interface between design and manufacturing is through design rules. However, this interface is facing many challenges such as an explosion of design rules, lack of accuracy, insufficient flexibility, and so on. On the other hand, model-based approaches require fast yet high fidelity metrics to guide layout optimizations. Which paradigms are best suited for the future routing - rules or models, gridded or grid-less routers? In terms of clock distribution, what are the design considerations that can minimize the impact of various sources of variations? This tutorial will cover different aspects of DFM-aware routing, and provide an introduction to contemporary high performance clocking, including a discussion of variation-aware clock design techniques.

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Cascade Ballroom

1:30pm - 5:30pm

Tutorial 5 - Modeling Deterministic Timing and Reliability Effects in Sub-65 nm Flows

Organizer: Noel Menezes - Intel Corp., Hillsboro, OR

Speakers: Satya Pullela - Clear Shape Technologies Inc., Santa Clara, CA
Chandramouli Kashyap - Intel Corp., Austin, TX
Bruce McGaughey - Cadence Design Systems, Inc., San Jose, CA

Description: Stringent power constraints and higher process and environmental variability have led to increased expectations in the accuracy of timing tools which are used to drive power optimization. Designers have come to expect silicon-level accuracy in static timing tools to achieve effective power-performance optimization. The first part of this tutorial deals with advances in the modeling of deterministic process and environmental variations in timing analysis flows. We will provide an in-depth analysis of the modeling of lithography-related deterministic process variations in timing, environmental effects like supply voltage, temperature, cross-capacitance, multiple-input switching, and modeling errors that arise from waveform abstraction, nonlinear input capacitances, library models, simulation artifacts, and inaccurate driver models. Apart from a discussion of the issues, recent advances in timing analysis and modeling which show promise in improving correlation between timing models and silicon will be covered. Examples of these are current source models which are capable of modeling most environmental effects and litho-driven models for handling process variation effects. An emerging variation driver impacting design is a class of reliability effects like negative bias temperature instability and hot carrier injection that affect advanced process technologies. These effects incur a large device degradation cost over the lifetime of a product thereby affecting the performance characteristics of a product in a unique manner. Unlike classic reliability effects which are usually dealt with in a correct-by-construction manner in design, mitigating the impact of NBTI and HCI requires cell-level detailed analysis tools. This tutorial provides an introduction to the underlying physics of these phenomena along with the detailed transistor- and cell-level models, and the methodologies used to analyze these effects in design flows.