

Tutorials .....9:00 AM - 5:00 PM	Registration .....8:00 AM - 10:00 AM
Continental Breakfast .....8:00 AM - 9:00 AM	Lunch .....12:00 PM - 1:00 PM

**Tutorial 1 - High Performance Integrated Circuit Analysis and Design Including On-Chip Inductance** Cedar Ballroom

Speakers: Chandramouli Kashyap - IBM Corp., Austin TX  
 Byron Krauter - IBM Corp., Austin, TX  
 Yehea I. Ismail - Northwestern Univ., Chicago, IL  
 Sachin Sapatnekar - Univ. of Minnesota, Minneapolis, MN

**Tutorial 2 - FPGAs: Computer-Aided Design, Applications and Future Architectures** Pine Ballroom

Speakers: Jeffrey Arnold - Stretch, Inc., Los Gatos, CA  
 Kia Bazargan - Univ. of Minnesota, Minneapolis, MN  
 Maya Gokhaleh - Los Alamos National Lab., Los Alamos, NM  
 Mark Jones - Virginia Tech, Blacksburg, VA  
 Alireza Kaviani - Xilinx, Inc., San Jose, CA

**Tutorial 3 - Specification and Design of Multimillion Gate SOCs** Fir Ballroom

Speakers: Ramesh Chandra - ST Microelectronics, San Diego, CA  
 Joerg Henkel - NEC USA, Inc., Princeton, NJ  
 Preeti Ranjan Panda - Indian Institute of Technology, Delhi, India  
 Sridevan Parameswaran - Univ. of New South Wales, New South Wales, Australia  
 Loganath Ramachandran - Synopsys, Inc., Mountain View, CA

**Tutorial 4 - Placement - the Key Problem in Physical Design** Oak Ballroom

Speakers: Jürgen Koehl - IBM Corp., Essex Junction, VT  
 John Lillis - Univ. of Illinois, Chicago, IL  
 Salil Raje - Hierarchical Design Inc., Santa Clara, CA  
 Jens Vygen - Univ. of Bonn, Bonn, Germany

# Thursday, November 14, 2002

ICCAD-2002

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## Tutorial 1 - High Performance Integrated Circuit Analysis and Design Including On-Chip Inductance

Cedar Ballroom

Speakers: Chandramouli Kashyap - *IBM Corp., Austin TX*  
Byron Krauter - *IBM Corp., Austin, TX*  
Yehea I. Ismail - *Northwestern Univ., Chicago, IL*  
Sachin Sapatnekar - *Univ. of Minnesota, Minneapolis, MN*

**Background:** On-chip inductance significantly affects the performance of chips in current technologies. These effects are expected to increase in future technologies due to several technology trends. Some of these trends are the exponentially increasing operating frequencies, lower resistivity interconnect (such as copper), low K dielectrics, faster devices (such as SOI and SiGe technologies), improved cooling techniques, and wider busses. The target audience consists of circuit designers, CAD engineers, and academic researchers. Familiarity with basic concepts in circuit design, model order reduction, extraction techniques, and design methodologies is assumed.

**Description:** The first part of the tutorial discusses the growing importance of on-chip inductance and its effects on propagation delay, rise time, power consumption, and noise. These effects are discussed both quantitatively and intuitively. This part also characterizes how important inductance effects are in current technologies.

The second part discusses the problem of inductance extraction. 3D full extraction techniques are discussed. Other techniques with lower computational complexity are also discussed such as 2<sub>D</sub> and 2<sub>D</sub>

extraction techniques and analytical approximate methods. The problem of determining the return paths is also discussed for these approximate techniques. The sensitivity of delay and performance estimations to errors in extracted inductance values is also discussed.

The third part discusses noise and inductive coupling effects. Wide busses are of specific interest. Model order reduction techniques that can efficiently handle multi-input circuits with large amount of coupling are also discussed. Realizable reduced order models are presented for RLC circuits.

The fourth part discusses design methodologies including inductance. Physical design and timing of integrated circuits including inductance is presented. The effects of inductance on repeater insertion, impedance matching, and wire and transistor sizing are discussed.

The fifth part discusses inductance effects in global distribution networks such as clock and power distribution networks.

Finally, future trends and expectations for inductance effects with technology scaling are discussed in the sixth part.

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Tutorial 2 - **FPGAs: Computer-Aided Design, Applications and Future Architectures**

Pine Ballroom

Speakers: Jeffrey Arnold - *Stretch, Inc., Los Gatos, CA*  
 Kia Bazargan - *Univ. of Minnesota, Minneapolis, MN*  
 Maya Gokhaleh - *Los Alamos National Lab., Los Alamos, NM*  
 Mark Jones - *Virginia Tech., Blacksburg, VA*  
 Alireza Kaviani - *Xilinx, Inc., San Jose, CA*

**Background:** With increasing system complexities and the need to reduce manufacturing costs, use of FPGAs in SOC designs is becoming inevitable. An FPGA component in SOC would increase fault tolerance and product durability, because the FPGA fabric can be tailor-made in the running environment of the system with new configurations to either overcome faults or reflect updates to the original design. This tutorial addresses issues that facilitate utilizing FPGAs in such a context. The target audience consists of circuit designers, CAD engineers and academic researchers.

**Description:** The first part of the tutorial covers existing and emerging commercial and academic FPGA architectures. We discuss the effects of different architectural options such as the granularity of functional units on the FPGA, size and physical distribution of memory modules within the FPGA fabric, embedding the FPGA fabric within an ASIC design or vice-versa, hierarchical structures and communication mechanisms for inter- and intra-FPGA data transfers.

The second part describes computer aided design methods for FPGAs, including synthesis, technology mapping, and physical design.

Different design effort / quality requirements at the development and the final optimization phases call for approaches that provide trade-offs between short design cycles and high clock frequencies. Higher quality expectations require interaction between synthesis and physical design. We also address the need for incremental design flows. Finally, we will address physical design algorithms that facilitate runtime reconfiguration of the FPGA fabric.

The third part surveys current C-to-hardware methods, including languages, compilation and high-level synthesis. Such methods are necessary for fast HW/SW co-design of large SOC designs. Memory block allocation in the FPGA fabric and resource allocation / scheduling will be discussed.

The fourth part will survey FPGA and reconfigurable computing applications that have shown significant improvements over ASIC implementations in terms of speed, power consumption and size. The present state and the future of dynamically reconfigurable systems will be discussed.

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### Tutorial 3 - Specification and Design of Multimillion Gate SOCs

Fir Ballroom

Speakers: Ramesh Chandra - *ST Microelectronics, San Diego, CA*  
Joerg Henkel - *NEC USA, Inc., Princeton, NJ*  
Preeti Ranjan Panda - *Indian Institute of Tech., New Delhi, India*  
Sridevan Parameswaran - *Univ. of New South Wales, New South Wales, Australia*  
Loganath Ramachandran - *Synopsys, Inc., Mountain View, CA*

**Background:** Advances in technology have made it possible to integrate several multi-million transistors on a single chip. However, design and verification teams face several challenges not been seen before: modeling and verifying entire system functionality, closing early on the system level architecture, extensive simulations of the hardware and software components and the final path to implementation of the entire SOC. New specification languages, new modeling and design paradigms, and new verification methods are evolving to meet these challenges.

**Description:** This tutorial will cover the state-of-the-art in specification and design methodologies. It will benefit design engineers, managers, researchers and students who are interested in understanding these new modeling, design and verification paradigms. This full-day tutorial is structured into five major parts.

- (a) System level design challenges from a designer's perspective
- (b) Specification languages for system level design
- (c) Functional and architectural modeling and verification
- (d) Platform based design concepts
- (e) Path from specification to implementation

An overview of the real challenges faced by system level designers will be presented with examples. The weaknesses of traditional design methods will be highlighted, thereby motivating the need for newer system level design tools and methodologies.

Several modeling languages that focus on system level have been proposed in the recent years. Languages such as SystemC, SpecC, and Superlog represent different approaches for specifying the entire system. In this section of the tutorial, we will present an overview of

these approaches, explain the specific properties of these languages and discuss in detail the application of various system modeling principles in SystemC.

In the next section of the tutorial we will focus on system level verification, which includes both functional and architectural verification. Functional verification addresses the modeling of the entire system functionality in order to understand system level performance issues. In general this requires heterogeneous modeling involving several models of computation. Architectural verification addresses architectural tradeoff issues that enable designers to close on the architecture early in the design cycle. This is achieved using transaction level models (TLMs) of the system components.

One popular method to manage SOC design complexity is to define a platform, which is an abstraction that embodies the lower level details. Such a platform along with an associated RTOS, forms the backbone for the SOC design. The next part of the tutorial will deal with the underlying concepts of platform-based design methodologies and their advantages compared to traditional system design concepts. Examples of commercial platforms will be presented.

The path to implementation from system level specification can be in any one of three domains: software; hardware; or hardware/software. In the software realization path, we will present modern compiler tools and techniques specifically targeted towards application specific systems. In the hardware section, we will present techniques for synthesis and discuss quality of results for designs created from system level specifications. Finally in the hardware/software implementation we will show the procedures that can lead to single/multi processor systems and ASIPs.

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Tutorial 4 - Placement - the Key Problem in Physical Design

Oak Ballroom

Speakers: Jürgen Koehl - *IBM Microelectronics, Essex Junction, VT*  
 John Lillis - *Univ. of Illinois, Chicago, IL*  
 Salil Rajee - *Hierarchical Design Inc., Santa Clara, CA*  
 Jens Vygen - *Univ. of Bonn, Bonn, Germany*

**Background:** Placement is one of the main tasks in physical layout. The quality of the placement becomes more and more important with shrinking feature sizes for several reasons: routability is harder to achieve; the wireload has an increasing impact on the timing behavior; and minimizing power consumption (which depends on the overall wire capacitance, and thus on the placement) is an increasingly important objective. However, even for the classical (and still useful) problem formulations, many questions have remained open. An additional challenge is posed by increasing complexities of chips, where placement has to deal with several million movable components.

The target audience includes design engineers, academic researchers, and anyone interested in physical design.

**Description:** This tutorial starts with a description of an automated design flow from a designer's viewpoint. The design objectives are discussed, and the key role of the placement problem, in interaction with other tasks like routing, timing optimization, logic changes and clocktree design, is stressed. Examples of current production parts and future trends highlight the design complexities that need to be supported. The first part ends with addressing the question of hierarchical versus flat design and illuminating some pros and cons.

The second part discusses hierarchy, and, in particular, floorplanning. We will discuss the two approaches to hierarchical physical implementation: one, the top-down floorplanning approach and two, the bottom-up partitioning approach. Key technologies that enable both approaches will be enumerated. We will discuss a few floorplan

representations and talk about algorithms used by current block placers. We will also talk about pin assignment techniques, and timing budgeting for hierarchical implementation.

Basic placement algorithms are subject of the third part of this tutorial. Classical formulations of the placement problem, though still useful, are far from being well-solved in spite of intensive research for decades. We will summarize what is known in theory, review the most successful placement approaches, and discuss their pros and cons. Stability and robustness is essential for achieving design closure when integrating other tools (like timing optimization) and objectives into the placement flow. While the classical and most common objective in global placement is minimization of some weighted netlength estimation, the goal in detailed placement (legalization) is usually rather to minimize the weighted total movement. We discuss both problems, their objectives, constraints, and solution techniques in theory and practice.

The effects of placement on the timing and routability properties of a circuit are paramount. The fourth part of this tutorial will give an overview of the state of knowledge in this area and will discuss potential future directions. Timing related topics will include performance models, path-based versus net-based timing optimization and implications of post-placement optimizations such as buffer insertion. In the routability area, congestion modeling and validation including constructive versus statistical models will be discussed. A discussion of global and detailed routability optimization techniques is also planned.