

Monday, November 11, 2002

ICCAD-2002

Registration - 7:00 AM - 5:00 PM (Bayshore Foyer)

Continental Breakfast - 7:00 AM (Sierra/Cascade Ballroom)

 videoed session

ICCAD Marketplace - 10:00 AM - 2:00 PM (Gateway Foyer)

Speakers' Breakfast - 7:30 AM (Monterey Room)

8:30  **OPENING SESSION: The Future of Electronic Games and the Impact on Design Automation**
 Chekib Akrouf - Director, Microprocessor Development, IBM Microelectronics, Austin, TX (Gateway Ballroom)

9:45

Coffee Break Sponsored by: 

	Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom
	SESSION 1A	SESSION 1B	SESSION 1C	SESSION 1D
10:30	Substrate Modeling	Invited Session: Design for Low-Power	Routing	Advances in Testing
12:00				
12:30				

12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)

	SESSION 2A	SESSION 2B	SESSION 2C
2:00	Novel Ideas in High Level Synthesis	Formal Techniques for Validation and Synthesis	Embedded Tutorial: Subthreshold Leakage Modeling and Reduction Techniques (Donner/Siskiyou Ballroom)
3:30			


Coffee Break

	SESSION 3A	SESSION 3B	SESSION 3C	SESSION 3D
4:00	Compilation Techniques for Hardware/Software Codesign	Timing-Driven Placement	 Invited Session: Emerging Technology Opportunities and Challenges	Inductance Modeling I
5:30				

 **MONDAYNIGHTPANEL: CAD FOR CAD'S SAKE? ARE CAD AND DESIGN DIVERGING?** 6:00 PM - 7:30 PM (Gateway Ballroom)




Tuesday, November 12, 2002

Registration - 7:00 AM - 5:00 PM (Bayshore Foyer)

Continental Breakfast - 7:00 AM (Sierra/Cascade Ballroom)  videoed session

ICCAD Marketplace - 10:00 AM - 2:00 PM (Gateway Foyer)

Speakers' Breakfast - 7:30 AM (Monterey Room)

Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom	
SESSION 4A	SESSION 4B	SESSION 4C	SESSION 4D	8:30
Efficient Simulation for Analog and RF	Interconnect Optimization	Chip-Level Communication Structures	New DFT Techniques and Methodologies	10:00
Coffee Break				
SESSION 5A	SESSION 5B	SESSION 5C	SESSION 5D	10:30
System-Level Analog Design	Inductance Modeling II	 Emerging Technologies: Circuits and Systems	Low Power and Transistor Level Optimization	12:00
12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)				
SESSION 6A	SESSION 6B	SESSION 6C		2:00
Statistical Techniques for Power and Timing Estimation	Embedded Tutorial: CAD Computation for Manufacturability: Can We Save VLSI Technology from	 Embedded Tutorial: Molecular Electronics: Devices, Systems and Tools for Gigagate, Gigabit Chips (Donner/Siskiyou Ballroom)		3:30
Coffee Break				
SESSION 7A	SESSION 7B	SESSION 7C	SESSION 7D	4:00
Satisfiability Checking	 Emerging Technologies: Device Modeling and Simulation	Circuit-Level Analog CAD	Physical Effects in Deep Sub Micron Technology	5:30
20TH ANNIVERSARY DINNER 6:00 PM (Sierra/Cascade Ballroom)				

Wednesday, November 13, 2002

ICCAD-2002

Registration - 7:00 AM - 5:00 PM (Bayshore Foyer)

Continental Breakfast - 7:00 AM (Sierra/Cascade Ballroom)

Speakers' Breakfast - 7:30 AM (Monterey Room)

 videoed session

	Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom
8:30	SESSION 8A	SESSION 8B	SESSION 8C	SESSION 8D
	Verification at the Switch, Gate and RT Levels	New Trends in Logic Synthesis	Memory Issues in High-Level Synthesis	Noise Effects on Circuit Operation
10:00	Coffee Break			
10:30	SESSION 9A	SESSION 9B	SESSION 9C	SESSION 9D
	Low Level Aware Behavioral Synthesis	Advances in Timing Analysis Accuracy	Customization of Embedded System Architectures	Advances in Combinational Synthesis
12:00	12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)			
12:30	12:00 - 2:00 Lunch Break (Sierra/Cascade Ballroom)			
2:00	SESSION 10A	SESSION 10B	SESSION 10C	SESSION 10D
	System-Level Performance and Power Modeling and Optimization	Advances in Dynamic Voltage Scheduling	Techniques in Placement	Model Order Reduction
3:30	Coffee Break			
4:00	SESSION 11A		SESSION 11B	
	Embedded Tutorial: SAT & ATPG: Boolean Engines for Formal Hardware Verification (Pine/Fir Ballroom)		Embedded Tutorial: The A to Z of SoCs (Donner/Siskiyou Ballroom)	
5:30				

Tutorials9:00 AM - 5:00 PM
 Continental Breakfast8:00 AM - 9:00 AM

Registration8:00 AM - 10:00 AM
 Lunch12:00 PM - 1:00 PM

- Tutorial 1 - High Performance Integrated Circuit Analysis and Design Including On-Chip Inductance** Cedar Ballroom
- Speakers: Chandramouli Kashyap - IBM Corp., Austin TX
 Byron Krauter - IBM Corp., Austin, TX
 Yehea I. Ismail - Northwestern Univ., Chicago, IL
 Sachin Sapatnekar - Univ. of Minnesota, Minneapolis, MN
- Tutorial 2 - FPGAs: Computer-Aided Design, Applications and Future Architectures** Pine Ballroom
- Speakers: Jeffrey Arnold - Stretch, Inc., Los Gatos, CA
 Kia Bazargan - Univ. of Minnesota, Minneapolis, MN
 Maya Gokhaleh - Los Alamos National Lab., Los Alamos, NM
 Mark Jones - Virginia Tech, Blacksburg, VA
 Alireza Kaviani - Xilinx, Inc., San Jose, CA
- Tutorial 3 - Specification and Design of Multimillion Gate SOCs** Fir Ballroom
- Speakers: Ramesh Chandra - ST Microelectronics, San Diego, CA
 Joerg Henkel - NEC USA, Inc., Princeton, NJ
 Preeti Ranjan Panda - Indian Institute of Technology, Delhi, India
 Sridevan Parameswaran - Univ. of New South Wales, New South Wales, Australia
 Loganath Ramachandran - Synopsys, Inc., Mountain View, CA
- Tutorial 4 - Placement - the Key Problem in Physical Design** Oak Ballroom
- Speakers: Jürgen Koehl - IBM Corp., Essex Junction, VT
 John Lillis - Univ. of Illinois, Chicago, IL
 Salil Raje - Hierarchical Design Inc., Santa Clara, CA
 Jens Vygen - Univ. of Bonn, Bonn, Germany

Monday, November 11, 2002

ICCAD-2002

Opening Session

 - Videoed Session

Time: 8:30 AM to 9:45 AM

Room: Gateway Ballroom

Opening Remarks

Lawrence T. Pileggi - ICCAD-2002 General Chair, Carnegie Mellon Univ., Pittsburgh, PA

Award Presentations

- William J. McCalla ICCAD Best Paper Award

This award is given in memory of William J. McCalla for his contributions to ICCAD and his CAD technical work throughout his career.

Paper 3D.1A [Local Circuit Topology for Inductance Parasitics](#) - Andrea Pacelli
presented Monday, November 11 at 4:00 PM in the Oak Ballroom.

Paper 8B.2 [Metrics for Structural Logic Synthesis](#) - Prabhakar Kudva, William Dougherty, Andrew Sullivan
presented Wednesday, November 13 at 8:30 AM in the Pine/Fir Ballroom.

Sponsored by:



- CAS Industrial Pioneer Award

Howard C. Yang - IDT-Newave Technology Co., Ltd. Shanghai, China

Citation: For pioneering development leading to high-volume production of mixed-signal products for the Chinese industry by co-founding Newave Technology Co., Ltd., the first IC design house in China to successfully develop mixed-signal ICs, and also for contributions to mixed-signal education in China through mixed-signal curriculum development, teaching, advising, and mentoring graduate students and faculty.

Presented by: IEEE CASS President-Elect - Giovanni De Micheli

- ACM/SIGDA CADathlon Program Contest Winners

CADathlon challenges students in their CAD knowledge, and their problem solving, programming, and teamwork skills.

Presented by: SIGDA Representative - Soha Hassoun ACM/SIGDA Chair - Robert Walker

Keynote • The Future of Electronic Games and the Impact on Design Automation

Chehib Akrouf - Director, Microprocessor Development, IBM Microelectronics, Austin, TX

Keynote: 🎮 - Videoed Session

The Future of Electronic Games and the Impact on Design Automation

Chekib Akrouit - Director, Microprocessor Development, IBM Microelectronics, Austin, TX

8:30 AM - 9:45 AM in the Gateway Ballroom

The electronic games phenomenon permeates our culture, evidenced by the fact that some 60% of all Americans -- more than 145 million people -- play computer and video games. It's serious business, it's growing, and it's here to stay. After the birth of Spacewar and Pong nearly 40 years ago, the games industry experienced an explosion in growth. The primary drivers of this extraordinary change have been the gamers' unquenchable desire for more realism, interaction, and mobility. To meet that market demand, the hardware developers were motivated to crank up the speed and bandwidth of the processor, increase the memory size and access time, and decrease power consumption -- all of which have serious implications for design automation. Today, correctly configured PCs and game consoles are a game developer's dream. With professional graphics engines handling the calculations to create the graphics, the microprocessor is left to focus on the calculations to create characters that behave more like real people and gaming environments that are more intense. DVD formats allow developers to include a deeper story line, richer graphics, sound, and video.

The future holds many challenges for the games industry. New technologies are required to be able to handle speech recognition, handwriting recognition, artificial intelligence, and video and audio streaming. Developers will consume every FLOP and memory byte available to make games that can provide automated generation of environments and characters. Wireless games will become more refined, and mobility will take on increased significance. Probably the most noteworthy trend will be the move toward broadband entertainment centers. Without a doubt, the impact on processor development, tools development, and design automation will be as enormous.

Until recently, wires have kept pace with transistors in scaled designs. The ITRS roadmap and our own experience shows that this is no longer true. This means that design systems have to give much more attention to wires. Doing so turns synthesis upside down, focusing on interconnect delays not just logic depth.

In the past, performance was most critical out of the triple constraints of performance, area and power. Today power is number one, while performance requirements must still be met. In other designs, performance is traded off for lower power but this is not possible for the electronic game industry because a certain amount of work is required to meet the "real time" performance requirements. In this new low power electronic game industry, new tools and methodologies for power management are necessary along with a higher emphasis on power savings from chip designers and architects. These tools range from power prediction to power grid distribution analysis. They provide critical feedback for designers to make proper choices in the design.

Chekib Akrouit Biography

Chekib Akrouit graduated with a BS in Physics from the University Pierre & Marie Curie in France, and then went on to obtain his PhD in Electronics and Physics. He joined IBM in 1982, where he worked on the bipolar high speed SRAM, then CMOS Cache Design for a high speed microprocessor. He managed several areas from microprocessors to ASICs to analog mixed signal design. At the present, Chekib is Director of high speed and broadband microprocessor development in IBM's Microelectronics Division, where he is responsible for PowerPC processors for Apple Macintosh and Nintendo Game Cube. He is also responsible for the Cell Project being developed through a Sony/Toshiba/IBM partnership in Austin, Texas.

Time: 10:30 AM to 12:00 PM

Room: Cedar

SESSION 1A SUBSTRATE MODELING

Moderators: Eli Chiprout - Intel Corp., Chandler, AZ
Sharad Kapur - Agere Systems, Inc., Murray Hill, NJ

Accurate and efficient modeling of the substrate has become critical for high frequency design. The first paper uses an efficient method to precompute Green's functions for use in a BEM for noise analysis. The second paper combines BEM and FEM methods to combine accuracy and efficiency for substrate modeling. The third paper describes a technique for augmenting inductance extraction in the presence of a lossy substrate.

1A.1 COMPREHENSIVE FREQUENCY-DEPENDENT SUBSTRATE NOISE ANALYSIS USING BOUNDARY ELEMENT METHODS

Hongmei Li (hli4@uiuc.edu), Jorge Carballido, Harry H. Yu, Vladimir I. Okhmatovski, Elyse Rosenbaum, Andreas C. Cangellaris - Univ. of Illinois, Urbana, IL

1A.2 THEORETICAL AND PRACTICAL VALIDATION OF COMBINED BEM/FEM SUBSTRATE RESISTANCE MODELING

Eelco Schrik (e.schrik@its.tudelft.nl), Patrick M. Dewilde, Nick P. van der Meijs - Delft Univ. of Tech., Delft, The Netherlands

1A.3 IMPLICIT TREATMENT OF SUBSTRATE AND POWER-GROUND LOSSES IN RETURN-LIMITED INDUCTANCE EXTRACTION

Dipak Sitaram - Cadence Design Systems, Inc., New Providence, NJ
Yu Zheng, Kenneth L. Shepard (shepard@ee.columbia.edu) - Columbia Univ., New York, NY

Time: 10:30 AM to 12:00 PM

Room: Pine/Fir

SESSION 1B INVITED SESSION: DESIGN FOR LOW-POWER

Moderators: Borivoje Nikolic - Univ. of California, Berkeley, CA
Lawrence T. Pileggi - Carnegie Mellon Univ., Pittsburgh, PA

Low power will soon become the primary design objective for enabling larger scale integration. The first paper explores multiple trade-offs to optimize power consumption from the application level to low-level device integration. The second paper elaborates on simultaneously tuning the supply and threshold voltage and the third paper considers the actual logic structure for power minimization through supply and threshold voltage adjustment and gate sizing.

1B.1 MINIMIZING POWER ACROSS MULTIPLE TECHNOLOGY AND DESIGN LEVELS

Takayasu Sakurai (tsakurai@iis.u-tokyo.ac.jp) - Univ. of Tokyo, Tokyo, Japan

1B.2 OPTIMIZATION AND CONTROL OF V_{DD} AND V_{TH} FOR LOW-POWER, HIGH-SPEED CMOS DESIGN

Tadahiro Kuroda (kuroda@elec.keio.ac.jp) - Keio Univ., Yokohama, Japan

1B.3 METHODS FOR TRUE POWER MINIMIZATION

Robert W. Brodersen - Univ. of Berkeley, Berkeley, CA
Mark A. Horowitz - Stanford Univ., Stanford, CA
Dejan Markovic, Borivoje Nikolic (bora@bwrc.eecs.berkeley.edu) - Univ. of California, Berkeley, CA
Vladimir Stojanovic - Stanford Univ., Stanford, CA

Time: 10:30 AM to 12:30 PM

Room: Donner/Siskiyou

SESSION 1C ROUTING

Moderators: Tong Gao - Monterey Design Systems, Sunnyvale, CA
Charles J. Alpert - IBM Corp., Austin, TX

As design sizes scale, routing becomes increasingly critical for achieving design closure. The first two papers in this session apply multilevel routing techniques to construct efficient solutions on large designs. The third paper proposes a method to reduce the runtime of global and detailed routing via intermediate track assignment. The final paper in the session proposes an ECO algorithm for minimizing design perturbations when the power grid is modified.

- 1C.1 **A NOVEL FRAMEWORK FOR MULTILEVEL ROUTING CONSIDERING ROUTIBILITY AND PERFORMANCE**
Yao Wen Chang (ywchang@cc.ee.ntu.edu.tw) - National Taiwan Univ., Taipei, Taiwan, ROC
Shih Ping Lin - National Chiao Tung Univ., Hsinchu, Taiwan, ROC
- 1C.2 **AN ENHANCED MULTILEVEL ROUTING SYSTEM**
Yan Zhang (zhangyan@cs.ucla.edu), Jason Cong, Min Xie - Univ. of California, Los Angeles, CA
- 1C.3 **TRACK ASSIGNMENT: A DESIRABLE INTERMEDIATE STEP BETWEEN GLOBAL ROUTING AND DETAILED ROUTING**
Shabbir H. Batterywala (battery@synopsys.com), Narendra Shenoy - Synopsys, Inc., Bangalore, India
William Nicholls - Synopsys, Inc., Hillsboro, OR
Hai Zhou - Northwestern Univ., Evanston, IL
- 1C.4 **ECO ALGORITHMS FOR REMOVING OVERLAPS BETWEEN POWER RAILS AND SIGNAL WIRES**
Hua Xiang (xiangh@cs.utexas.edu) - Univ. of Illinois, Urbana, IL
Kai-Yuan Chao - Intel Corp., Austin, TX
D. F. Wong - Univ. of Illinois, Urbana, IL

Time: 10:30 AM to 12:30 PM

Room: Oak

SESSION 1D ADVANCES IN TESTING

Moderators: Tomoo Inoue - Hiroshima City Univ., Hiroshima, Japan
M. Jeske-Chrzanowska - Portland Univ., Portland, OR

This session addresses the following four topics: fast seed computation for test pattern compression, the definition of undetectable faults in partial scan, enhancements in deterministic test pattern generation, and some considerations in path selection for delay testing.

- 1D.1 **FAST SEED COMPUTATION FOR RESEEDING SHIFT REGISTER IN TEST PATTERN COMPRESSION**
Nahmsuk Oh (nahmsuk@synopsys.com), Rohit Kapur, Thomas W. Williams - Synopsys, Inc., Mountain View, CA
- 1D.2 **ON UNDETECTABLE FAULTS IN PARTIAL SCAN CIRCUITS**
Irith Pomeranz (pomeranz@ecn.purdue.edu)- Purdue Univ., West Lafayette, IN
Sudhakar M. Reddy - Univ. of Iowa, Iowa City, IA
- 1D.3 **CONFLICT DRIVEN TECHNIQUES FOR IMPROVING DETERMINISTIC TEST PATTERN GENERATION**
Chen Wang (cwang@eng.uiowa.edu), Sudhakar M. Reddy - Univ. of Iowa, Iowa City, IA
Irith Pomeranz - Purdue Univ., West Lafayette, IN
Xijiang Lin, Janusz Rajski - Mentor Graphics Corp., Wilsonville, OR
- 1D.4 **ON THEORETICAL AND PRACTICAL CONSIDERATIONS OF PATH SELECTION FOR DELAY FAULT TESTING**
Jing Jia Liou, Li C. Wang (licwang@ece.ucsb.edu), Tim Cheng - Univ. of California, Santa Barbara, CA

Time: 2:00 PM to 3:30 PM

Room: Cedar

SESSION 2A NOVEL IDEAS IN HIGH LEVEL SYNTHESIS

Moderators: Julio L. da Silva - Get2Chip.com, Inc., San Jose, CA
Patrick R. Schaumont - Univ. of California,
Los Angeles, CA

The three papers in this session present new problem formulations and solutions in high level synthesis. The first paper defines a concise expression of dynamic circuit reconfiguration by means of a type system. The second paper presents a power-optimization method starting from the RTL description of a system by using net switching activity reduction. Finally, the third paper presents a new formulation addressing predictability in high level synthesis.

2A.1 INTERFACE SPECIFICATION FOR RECONFIGURABLE COMPONENTS

Satnam Singh (satnam.singh@xilinx.com) - Xilinx, Inc.,
San Jose, CA

2A.2 INTERCONNECT-AWARE HIGH-LEVEL SYNTHESIS FOR LOW POWER

Lin Zhong (lzhong@princeton.edu), Niraj K. Jha -
Princeton Univ., Princeton, NJ

2A.3 PREDICTABILITY: DEFINITION, ANALYSIS AND OPTIMIZATION

Ankur Srivastava (apple@cs.ucla.edu) - Univ. of Maryland,
College Park, MD
Majid Sarrafzadeh - Univ. of California, Los Angeles, CA

Time: 2:00 PM to 3:30 PM

Room: Pine / Fir

SESSION 2B FORMAL TECHNIQUES FOR VALIDATION AND SYNTHESIS

Moderators: Aarti Gupta - NEC USA, Inc., Princeton, NJ
Rajeev Ranjan - Real Intent, Santa Clara, CA

This session describes applications of formal techniques in some non-traditional settings. The first describes its use in solving constraints for faster generation of simulation vectors for functional validation. The second uses a maximization search over the Boolean space to derive imprecision errors in fixed-point arithmetic circuits. The last paper turns the problem of verifying compatible interfaces into one of synthesizing a converter using automata and game-theoretic ideas.

2B.1 SYMPLIFYING BOOLEAN CONSTRAINT SOLVING IN RANDOM SIMULATION-VECTOR GENERATION

Jun Yuan (jun.yuan@motorola.com), Ken Albin -
Motorola, Austin, TX
Adnan Aziz - Univ. of Texas, Austin, TX
Carl Pixley - Synopsys, Inc., Hillsboro, OR

2B.2 SPECIFYING AND VERIFYING IMPRECISE SEQUENTIAL DATAPATHS BY ARITHMETIC TRANSFORMS

Katarzyna Radecka - Concordia Univ., Montreal, PQ, Canada
Zeljko Zilic (zeljko@macs.ece.mcgill.ca) - McGill Univ.,
Montreal, PQ, Canada

2B.3 CONVERTIBILITY VERIFICATION AND CONVERTER SYNTHESIS: TWO FACES OF THE SAME COIN

Roberto Passerone (robp@cadence.com) -
Cadence Design Systems, Inc., Berkeley, CA
Luca de Alfaro - Univ. of California, Santa Cruz, CA

Time: 2:00 PM to 3:30 PM

Room: Donner/Siskiyou

**SESSION 26 EMBEDDED TUTORIAL: SUBTHRESHOLD
LEAKAGE MODELING AND REDUCTION TECHNIQUES**

Moderators: Georges Gielen - Katholieke Univ., Leuven, Belgium
Farid N. Najm - Univ. of Toronto, Toronto, ON, Canada

As technology scales, subthreshold leakage currents grow exponentially and become an increasingly large component of total power dissipation. CAD tools to help model and manage subthreshold leakage currents will be required to develop ultra low power and high performance integrated circuits. This tutorial gives an overview of current research directions to control leakage currents, with an emphasis on areas where CAD improvements will be needed. The first part of this tutorial explores techniques to model subthreshold leakage currents at the device, circuit, and system levels. It is important to develop methods to predict these leakage currents accurately and efficiently in order to manage overall power consumption. The second part of this tutorial develops circuit techniques to control subthreshold leakage currents in both the standby and active states. Standby leakage reduction is especially important in portable burst mode applications where systems remain in idle states for long periods of time. A broad overview of standby leakage reduction techniques is described, including current research areas such as source biasing, dual Vt partitioning, MTCMOS, and VTCMOS. As technology scales even further, active leakage reduction becomes important as well. This tutorial finally explores ways to reduce total active power by limiting leakage currents and optimally trading off between dynamic and leakage power components.

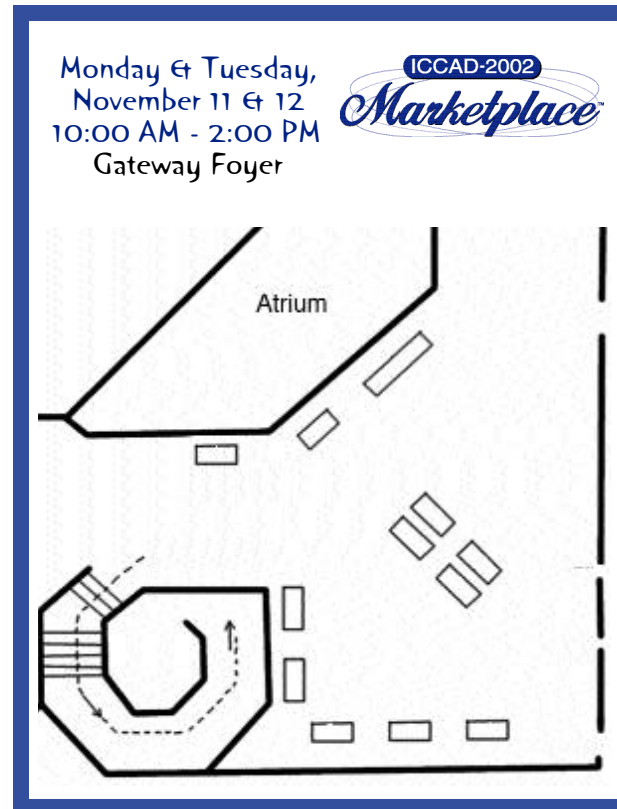
Presenter:

James Kao - Silicon Labs., Austin, TX

Co-Authors:

Anantha Chandrakasan - Massachusetts Institute of Tech.,
Cambridge, MA

Siva Narendra - Intel Corp., Hillsboro, OR



Time: 4:00 PM to 5:30 PM

Room: Cedar

SESSION 3A COMPILATION TECHNIQUES FOR HARDWARE/SOFTWARE CODESIGN

Moderators: Joerg Henkel - NEC USA, Inc., Princeton, NJ
Luc Semeria - Synopsys, Inc., Mountain View, CA

This session addresses compiler smarts to help the hardware/software codesign process. The first paper presents a number of dynamic recompilation techniques targeting power optimization. The second paper discusses a BDD based pointer analysis technique which is crucial for compiling high-level programs into hardware. The third paper takes on the counter-intuitive idea of hw/sw partitioning at the level of assembly code.

- 3A.1 **SYMBOLIC POINTER ANALYSIS**
Jianwen Zhu (jzhu@eecg.toronto.edu) - Univ. of Toronto,
Toronto, ON, Canada
- 3A.2 **DYNAMIC COMPILATION FOR ENERGY ADAPTATION**
Priya Unnikrishnan, Guangyu Chen, Mahmut Kandemir
(kandemir@cse.psu.edu), David R. Mudgett - Penn State Univ.,
University Park, PA
- 3A.3 **HARDWARE/SOFTWARE PARTITIONING
OF SOFTWARE BINARIES**
Greg M. Stitt (gstitt@cs.ucr.edu), Frank Vahid - Univ. of
California, Riverside, CA

Time: 4:00 PM to 5:30 PM

Room: Pine/Fir

SESSION 3B TIMING-DRIVEN PLACEMENT

Moderators: Rajeev Jayaraman - Xilinx, Inc., San Jose, CA
Jens Vygen - Bonn Univ., Bonn, Germany

This session presents new advances in timing-driven placement and partitioning, including a novel path-counting based net-weighting scheme, a delay-budgeting method based on design hierarchy, and cutsize and path-based delay trade-off in circuit partitioning.

- 3B.1 **A NOVEL NET WEIGHTING ALGORITHM
FOR TIMING-DRIVEN PLACEMENT**
Tianming Kong (kongtm@cs.ucla.edu)- Aplus Design Tech.,
Inc., Los Angeles, CA
- 3B.2 **TIMING-DRIVEN PLACEMENT USING DESIGN HIERARCHY GUIDED
CONSTRAINT GENERATION**
Xiaojian X. Yang (xjyang@cs.ucla.edu), Bo-Kyung Choi,
Majid Sarrafzadeh - Univ. of California, Los Angeles, CA
- 3B.3 **MULTI-OBJECTIVE CIRCUIT PARTITIONING FOR CUTSIZE AND
PATH-BASED DELAY MINIMIZATION**
Cristinel Ababei, Selvakkumaran Navaratnasothie,
Kia Bazargan (kia@ece.umn.edu), George Karypis -
Univ. of Minnesota, Minneapolis, MN

Time: 4:00 PM to 5:30 PM

SESSION 3C



- Videoed Session

Room: Donner/Siskiyou

INVITED SESSION: EMERGING TECHNOLOGY OPPORTUNITIES AND CHALLENGES

Moderators: Makoto Ikeda - Univ. of Tokyo, Tokyo, Japan
 Andreas Kuehlmann - Cadence Berkeley Labs., Berkeley, CA

Advancements in semiconductor technologies provide novel integration opportunities but also uncharted challenges for an automated design and verification flow. The first paper presents the features of a newly developed, hybrid ASIC/FPGA chip architecture and elaborates on open CAD problems for its automated design. The second papers describes the use of voltage islands for power management and the third paper elaborates on CAD challenges for the next-generation semiconductor technologies.

3C.1 A HYBRID ASIC AND FPGA ARCHITECTURE

Paul S. Zuchowski (paulz@us.ibm.com), Christopher Reynolds, Rick J. Grupp - IBM Microelectronics, Essex Junction, VT
 Shelly G. Davis - Xilinx, Inc., San Jose, CA
 Brendan Creman - Xilinx, Inc., Dublin, Ireland
 Bill Troxel - Xilinx, Inc., Boulder, CO

3C.2 MANAGING POWER AND PERFORMANCE FOR SYSTEM-ON-CHIP DESIGNS USING VOLTAGE ISLANDS

David E. Lackey (delacke@us.ibm.com), Scott Gould, Thomas R. Bednar, John Cohn, Paul S. Zuchowski - IBM Microelectronics, Essex Junction, VT

3C.3 SUB-90nm TECHNOLOGIES—CHALLENGES AND OPPORTUNITIES FOR CAD

Tanay Karnik, Shekhar Borkar (shekhar.y.borkar@intel.com), Vivek De - Intel Corp., Hillsboro, OR

Time: 4:00 PM to 5:30 PM

SESSION 3D INDUCTANCE MODELING I

Room: Oak

Moderators: Eli Chiprout - Intel Corp., Chandler, AZ
 Mustafa Celik - Magma Design Automation, Inc., Cupertino, CA

Inductance extraction for full-chip analysis is complex and CPU intensive, but becoming important. The first paper takes a new direction by generating circuit models based on the scalar and vector potentials. The second paper proposes changes to the K-method and creates an inductance-aware simulation environment. The final paper proposes to apply precorrected-FFT to inductance extraction.

3D.1 BEST PAPER - A LOCAL CIRCUIT TOPOLOGY FOR INDUCTIVE PARASITICS

Andrea Pacelli (pacelli@ece.sunysb.edu) - State Univ. of New York, Stony Brook, NY

3D.2 INDUCTWISE: INDUCTANCE-WISE INTERCONNECT SIMULATOR AND EXTRACTOR

Tsung Hao Chen (tchen@cae.wisc.edu), Clement Luk, Hyungsuk Kim, Charlie Chung Ping Chen - Univ. of Wisconsin, Madison, WI

3D.3 A PRECORRECTED-FFT METHOD FOR SIMULATING ON-CHIP INDUCTANCE

Haitian Hu - Univ. of Minnesota, Minneapolis, MN
 David Blaauw - Univ. of Michigan, Ann Arbor, MI
 Vladimir Zolotov, Kaushik Gala, Min Zhao, Rajendran Panda - Motorola, Inc., Austin, TX
 Sachin S. Sapatnekar (sachin@ece.umn.edu) - Univ. of Minnesota, Minneapolis, MN

Monday, November 11, 2002

ICCAD-2002

Time: 6:00 PM to 7:30 PM

Room: Gateway Ballroom

MONDAY NIGHT PANEL  - Videod Session
CAD FOR CAD'S SAKE? ARE CAD AND DESIGN DIVERGING?

Moderator: John Cohn - IBM Microelectronics, Essex Junction, VT

In the beginning, CAD tools were written by designers to reduce the tedium of jobs like cutting out photomask data from plastic film. We've come a long way since the first designer put down the Xacto knife and picked up a light pen. CAD is now a multi-billion dollar industry with its own conferences, its own heroes, and its own ideas. No one can deny that CAD innovation has been one of the prime drivers of the microelectronics revolution. Still, a common criticism today is that CAD has drifted away from its design roots. We live in a time when few CAD engineers have ever designed a chip. Should we be taking more direction from the design community... or is our job to lead them? Remember some innovations such as logic synthesis were initially met with fierce resistance from designers.

Whomever is in charge, are we tackling the problems that will enable designers to push their industry, or are we growing too introspective and working on the problems of our own creation?

With CAD conferences filling with discussions of databases and incremental improvements to long solved problems, maybe it's time to step back and ask ourselves... 'Are CAD and design diverging?' This panel will explore that question from both the designer's and CAD engineer's perspective. Please come prepared to share your thoughts.

Panelists:

Shekhar Borkar - Intel Corp., Hillsboro, OR
Mark Horowitz - Stanford Univ., Stanford CA
Chekib Akrouf - IBM Microelectronics, Austin TX
Don MacMillan - Synopsys, Inc., Mountain View, CA
Rob A. Rutenbar - Carnegie Mellon Univ., Pittsburgh PA
Steve Teig - Cadence Design Systems, Inc., Santa Clara, CA

Time: 8:30 AM to 10:00 AM

Room: Cedar

SESSION 4A EFFICIENT SIMULATION FOR ANALOG AND RF

Moderators: Helmut E. Graeb - Technical Univ. of Munich,
Munich, Germany
Ken Kundert - Cadence Design Systems, Inc., San Jose,
CA

Verification tools are central to the design of all high-performance analog and RF. Many critical designs remain difficult (or impossible) to simulate well. This session shows three important advances in this area. The first paper analyzes the differences between two current strategies for evaluating oscillator phase noise. The second paper describes an efficient behavioral simulation tool for continuous time delta-sigma modulators. The final paper describes new numerical techniques to make Fourier-envelope simulation robust.

4A.1 ON THE DIFFERENCE BETWEEN TWO WIDELY PUBLICIZED METHODS FOR ANALYZING OSCILLATOR PHASE BEHAVIOR

Piet Vanassche (piet.vanassche@esat.kuleuven.ac.be),
Georges Gielen, Willy Sansen - Katholieke Univ.,
Leuven, Belgium

4A.2 A BEHAVIORAL SIMULATION TOOL FOR CONTINUOUS-TIME DELTA-SIGMA MODULATORS

Kenneth Francken (francken@ieee.org), Martin Vogels, Ewout
Martens, Georges Gielen - Katholieke Univ., Leuven, Belgium

4A.3 MAKING FOURIER-ENVELOPE SIMULATION ROBUST

Jaijeet Roychowdhury (jr@ece.umn.edu) -
Univ. of Minnesota, Minneapolis, MN

Time: 8:30 AM to 10:00 AM

Room: Pine/Fir

SESSION 4B INTERCONNECT OPTIMIZATION

Moderators: Cheng-Kok Koh - Purdue Univ., West Lafayette, IN
Charles Chiang - Synopsys, Inc., Mountain View, CA

Various interconnect optimizations are useful to achieve timing closure, synchronize asynchronous clock domains, and improve reliability and manufacturability. The first paper addresses the problem of constructing buffered routing paths for multiple clock domains. The second paper presents the optimal wire shaping function for electromigration, and the final paper discusses single net routing for reliability improvement.

4B.1 OPTIMAL BUFFERED ROUTING PATH CONSTRUCTIONS FOR SINGLE AND MULTIPLE CLOCK DOMAIN SYSTEMS

Soha Hassoun (soha@eeecs.tufts.edu) - Tufts Univ.,
Medford, MA
Charles J. Alpert - IBM Corp., Austin, TX
Meera Thiagarajan - Tufts Univ., Medford, MA

4B.2 SHAPING INTERCONNECT FOR UNIFORM CURRENT DENSITY

Muzhou Shao (mushao@cs.utexas.edu) - Univ. of Texas,
Austin, TX
D. F. Wong - Univ. of Illinois, Urbana, IL
Youxin Gao, Li-Pen Yuan - Synopsys, Inc., Mountain View, CA
Huijing Cao - Motorola, Inc., Tianjin, China

4B.3 NON-TREE ROUTING FOR RELIABILITY AND YIELD IMPROVEMENT

Andrew B. Kahng, Bao Liu, Ion Mandoiu
(mandoiu@cs.ucsd.edu) - Univ. of California,

Time: 8:30 AM to 10:00 AM

Room: Donner/Siskiyou

SESSION 4C CHIP-LEVEL COMMUNICATION STRUCTURES

Moderators: Leon Stok - IBM Corp., Yorktown Heights, NY
Dwight Hill - Synopsys, Inc., Mountain View, CA

Chip level performance is increasingly dominated by interblock communication. Even with optimal buffering it is impossible for a signal to traverse the chip in one cycle. These trends require a fresh approach to analysis and design of chip level interconnect.

4C.1 CONCURRENT FLIP-FLOP AND REPEATER INSERTION FOR HIGH PERFORMANCE INTEGRATED CIRCUITS

Pasquale Cocchini (pasquale.cocchini@intel.com) - Intel Corp., Hillsboro, OR

4C.2 THROUGHPUT-DRIVEN IC COMMUNICATION FABRIC SYNTHESIS

Tao Lin (tl@ece.cmu.edu), Lawrence T. Pileggi - Carnegie Mellon Univ., Pittsburgh, PA

4C.3 REPEATER INSERTION AND WIRE SIZING OPTIMIZATION FOR THROUGHPUT-CENTRIC VLSI GLOBAL INTERCONNECTS

Harshit Shah, Jeff A. Davis (jeff@ece.gatech.edu), Pun H. Shiu, Brian Bell, Namrata Sopory - Georgia Institute of Tech., Atlanta, GA

Time: 8:30 AM to 10:00 AM

Room: Oak

SESSION 4D NEW DFT TECHNIQUES AND METHODOLOGIES

Moderators: Bozena Kaminska - 3MT Solutions, Lake Oswego, OR
Tomoo Inoue - Hiroshima City Univ., Hiroshima, Japan

This session deals with test approaches for SoC ranging from a hierarchical DfT insertion, through logic BIST based on spectral information to low power scan architecture.

4D.1 TEST-MODEL BASED HIERARCHICAL DFT SYNTHESIS

Sanjay Ramnath (sramnath@synopsys.com), Frederic Neveux, Mokhtar Hirech, Felix Ng - Synopsys, Inc., Mountain View, CA

4D.2 CHARACTERISTIC FAULTS AND SPECTRAL INFORMATION FOR LOGIC BIST

Xiaoding Chen (xiaoding@visc.vt.edu), Michael S. Hsiao - Virginia Tech., Blacksburg, VA

4D.3 A NOVEL SCAN ARCHITECTURE FOR POWER-EFFICIENT, RAPID TEST

Ozgur Sinanoglu (ozgur@cs.ucsd.edu), Alex Orailoglu - Univ. of California at San Diego, La Jolla, CA

Time: 10:30 AM to 12:00 PM

Room: Cedar

SESSION 5A SYSTEM-LEVEL ANALOG DESIGN

Moderators: Jaijeet Roychowdhury - Univ. of Minnesota,
Minneapolis, MN

Henry Chang - Cadence Design Systems, Inc., San Jose, CA

Design of complex analog circuits is already challenging; design of complete analog and mixed-signal systems is even more difficult. This session presents three system-level analog design examples, and highlights both novel design methodologies and novel point tools. The first paper describes optimization of an integrated GPS receiver. The second paper presents a case study of substrate noise mitigation for a single-chip RF transceiver. The third paper describes an extension of convex programming methods to the design of pipelined A/D converters.

5A.1 OPTIMIZATION OF A FULLY INTEGRATED LOW POWER CMOS GPS RECEIVER

Philippe Coppejans, Wouter De Cock
(decocw@esat.kuleuven.ac.be), Paul Leroux,
Michiel Steyaert - Katholieke Univ., Leuven, Belgium

5A.2 ANALYSIS AND OPTIMIZATION OF SUBSTRATE NOISE COUPLING IN SINGLE-CHIP RF TRANSCEIVER DESIGN

Adil Koukab (adil.koukab@epfl.ch) - Swiss Federal
Univ. of Tech., Lausanne, Switzerland
Kaustav Banerjee - Univ. of California, Santa Barbara, CA
Michel Declercq - Swiss Federal Institute of Tech.,
Lausanne, Switzerland

5A.3 DESIGN OF PIPELINE ANALOG-TO-DIGITAL CONVERTERS VIA GEOMETRIC PROGRAMMING

Maria del mar Hershenson
(mar.hershensone@barcelonadesign.com) -
Barcelona Design, Inc. Newark, CA

Time: 10:30 AM to 12:00 PM

Room: Pine/Fir

SESSION 5B INDUCTANCE MODELING II

Moderators: Kenneth L. Shepard - Columbia Univ., New York, NY
Mattan Kamon - Coventor, Inc., Cambridge, MA

This session considers techniques for the high-frequency modeling of on-chip wires and packages. The first paper considers a technique for numerically generating a set of efficient basis functions for capturing skin and proximity effects. The second paper deals with transmission lines effects in the design of clock trees. The session ends with a new approach to building an equivalent RLC circuit structure with a windowed inductance matrix.

5B.1 PROXIMITY TEMPLATES FOR MODELING OF SKIN AND PROXIMITY EFFECTS ON PACKAGES AND HIGH FREQUENCY INTERCONNECT

Luca Daniel (dluca@eecs.berkeley.edu), Alberto L.
Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA
Jacob K. White - Massachusetts Institute of Tech.,
Cambridge, MA

5B.2 TRANSMISSION LINE DESIGN OF CLOCK TREES

Rafael E. Escovar (rafael_escovar@mentor.com), Robert Suaya -
Mentor Graphics Corp., Meylan, France

5B.3 ON-CHIP INTERCONNECT MODELING BY WIRE DUPLICATION

Guoan Zhong (zhongg@purdue.edu), Cheng-Kok Koh,
Kaushik Roy - Purdue Univ., West Lafayette, IN

Time: 10:30 AM to 12:30 PM

Room: Donner/Siskiyou

SESSION 5C  - Videoed Session

EMERGING TECHNOLOGIES: CIRCUITS AND SYSTEMS

Moderators: Mary Ann Maher - MEMSCAP Inc., Oakland, CA
Michael Butts - Cadence Design Systems, Inc., Portland, OR

This session focuses on architectures and representations for the design of MEMS and nanotechnology. The first paper presents an architecture for CMOS/nano co-design. The second paper presents methods to synthesize reversible logic with applications to quantum computation. The third paper introduces extraction and LVS techniques for design verification of integrated MEMS. The fourth paper describes a schematic-based lumped parameter circuit simulation approach for MEMS design.

- 5C.1 A CASE FOR CMOS/NANO CO-DESIGN
Matt M. Ziegler (ziegler@virginia.edu), Mircea R. Stan - Univ. of Virginia, Charlottesville, VA
- 5C.2 REVERSIBLE LOGIC CIRCUIT SYNTHESIS
Vivek V. Shende (vshende@umich.edu), Aditya K. Prasad, Igor L. Markov, John P. Hayes - Univ. of Michigan, Ann Arbor, MI
- 5C.3 EXTRACTION AND LVS FOR MIXED-DOMAIN INTEGRATED MEMS LAYOUTS
Bikram Baidya (bbaidya@ece.cmu.edu), Tamal Mukherjee - Carnegie Mellon Univ., Pittsburgh, PA
- 5C.4 SCHEMATIC-BASED LUMPED PARAMETERIZED BEHAVIORAL MODELING FOR SUSPENDED MEMS
Qi Jing (qjing@ece.cmu.edu), Tamal Mukherjee, Gary Fedder - Carnegie Mellon Univ., Pittsburgh, PA

Time: 10:30 AM to 12:30 PM

Room: Oak

SESSION 5D LOW POWER AND TRANSISTOR LEVEL OPTIMIZATION

Moderators: Rajeev Murgai - Fujitsu Labs. of America, Sunnyvale, CA
Michel Berklaar - Magma Design Automation, Inc., Eindhoven, The Netherlands

Low power has become an issue since the last generation of designs. Shrinking geometries and lower voltage threshold is making leakage power an increasing problem. The first three papers of this session address low power optimization, including leakage power. The last paper presents an improvement on analytical transistor sizing.

- 5D.1 STANDBY POWER OPTIMIZATION VIA TRANSISTOR SIZING AND DUAL THRESHOLD VOLTAGE ASSIGNMENT
Mahesh C. Ketkar (ketkar@ece.umn.edu), Sachin S. Sapatnekar - Univ. of Minnesota, Minneapolis, MN
- 5D.2 POWER EFFICIENCY OF VOLTAGE SCALING IN MULTIPLE CLOCK, MULTIPLE VOLTAGE CORES
Anoop Iyer, Diana Marculescu (dianam@ece.cmu.edu) - Carnegie Mellon Univ., Pittsburgh, PA
- 5D.3 OPTIMIZED POWER-DELAY CURVE GENERATION FOR STANDARD CELL ICs
Miodrag Vujkovic (miodrag@ee.washington.edu), Carl Sechen - Univ. of Washington, Seattle, WA
- 5D.4 GATE SIZING USING LAGRANGIAN RELAXATION COMBINED WITH A FAST GRADIENT-BASED PRE-PROCESSING STEP
Hiran K. Tennakoon (hiran@ee.washington.edu), Carl Sechen - Univ. of Washington, Seattle, WA

Time: 2:00 PM to 3:30 PM

Room: Cedar

SESSION 6A STATISTICAL TECHNIQUES FOR POWER AND TIMING ESTIMATION

Moderators: Farid N. Najm - Univ. of Toronto, Toronto, ON, Canada
Dennis M. Sylvester - Univ. of Michigan, Ann Arbor, MI

This session brings new statistical techniques to the issues of power consumption and noise-induced delay. The first two papers address circuit-level power modeling for building both average and cycle-accurate power models for logic blocks. The third paper propagates delay statistics while considering coupling noise.

6A.1 A MARKOV CHAIN SEQUENCE GENERATOR FOR POWER MACROMODELING

Xun Liu (xunliu@eecs.umich.edu), Marios C. Papaefthymiou -
Univ. of Michigan, Ann Arbor, MI

6A.2 CIRCUIT POWER ESTIMATION USING PATTERN RECOGNITION TECHNIQUES

Lipeng Cao (lipeng.cao@motorola.com) - Motorola, Inc.,
Austin, TX

6A.3 ESTIMATION OF SIGNAL ARRIVAL TIMES IN THE PRESENCE OF DELAY NOISE

Sarvesh Bhardwaj, Sarma B. Vrudhula
(sarma@ece.arizona.edu) - Univ. of Arizona, Tucson, AZ
David Blaauw - Univ. of Michigan, Ann Arbor, MI

Time: 2:00 PM to 3:30 PM

Room: Pine/Fir

SESSION 6B EMBEDDED TUTORIAL: CAD COMPUTATION FOR MANUFACTURABILITY: CAN WE SAVE VLSI TECHNOLOGY FROM ITSELF?

Moderators: Andrzej Strojwas - Carnegie Mellon Univ., Pittsburgh, PA
Andrew B. Kahng - Univ. of California at San Diego,
La Jolla, CA

Every 18 to 24 months, the areal density of VLSI doubles and the predicted date for the End of CMOS Scaling is pushed out approximately 18 to 24 months. This rate of growth has been controlled mainly by the increasing capabilities of lithographic patterning. However, the rate of improvement of lithography systems in key physical parameters such as illumination wavelength has begun to slow. To make up the shortfall, lithography has increasingly turned to using CAD tools to transform the geometric shapes in designs into shapes on photomasks which have been compensated for systematic pattern-distorting effects. As the requirements for this compensation grow, however, it becomes increasingly difficult to hide in post-tapeout data preparation, and must be considered in back-end design tools and methodologies.

This presentation will describe a number of the challenges to lithographic patterning, highlighting the factors that limit "physical scaling" and introduce the layout-to-mask shape transformations that compensate for these limitations. It will then describe the implementation of these transformations in general-purpose and specialized CAD tools, pointing out challenges like growth of computation effort. Finally, the presentation will describe how limitations of post-tapeout compensation drive the need for 'litho-aware' physical design tools, showing examples in cell design, place-and-route, and layout migration.

Presenters:

Mark Lavin - IBM Corp., Yorktown Heights, NY
Lars Liebman - IBM Corp., Yorktown Heights, NY

Time: 2:00 PM to 3:30 PM

Room: Donner/Siskiyou

SESSION 6C  - Videoed Session

EMBEDDED TUTORIAL: MOLECULAR ELECTRONICS: DEVICES, SYSTEMS
AND TOOLS FOR GIGAGATE, GIGABIT CHIPS

Moderators: Paul D. Franzon - North Carolina State Univ., Raleigh, NC
Tamal Mukherjee - Carnegie Mellon Univ., Pittsburgh,
PA

A new technology for digital electronics is emerging, with features in the 1 to 50 nanometer range, called nanoelectronics. Its molecular-scale devices and interconnects are made with carbon nanotubes, single-crystal semiconductor nanowires, and bistable organic molecules, self-assembled on silicon substrates. This tutorial seeks to inform the ICCAD community on how nanoelectronics technology is taking shape and where ICCAD research is needed.

Last year's ICCAD keynote speech and evening panel were on Nanotechnology and Information. The AAAS journal, Science, chose nanocircuits as its Breakthrough of the Year for 2001. Exciting results in basic research on molecular-scale electronic devices and interconnects are being reported with ever-greater frequency. Self-assembling digital systems with billions of components may become an engineering possibility in this decade. Impact on electronics, and ICCAD tools in particular, would be profound.

Nanoelectronic devices actually operating today in chemistry and physics labs include FETs, junction transistors and diodes, molecular switches, and mechanical switches. Logic gates with voltage gain

have been built. Some of these devices are programmable and non-volatile. Researchers project densities of 10^{11} to 10^{12} devices/cm². (In comparison, the 2001 ITRS roadmap for ASICs and MPUs projects 3×10^7 transistors/cm² for 2016.) Nanoelectronic fabrication would be bottom-up batch chemical and physical processes, forming semi-regular arrays with 1% to 5% defect rates. Circuit function would be programmed in and defects programmed around. Cheap gigagate, gigabit, gigaHertz, non-volatile FPGAs and RAMs, built with nanoelectronic arrays on microelectronic silicon substrates, may be in commercial production by 2010-2015.

Our tutorial has three parts: Part 1 surveys recent research results in nanoelectronic materials and devices and assembly techniques. Part 2 reports on initial published forays into how we might build nanoelectronic systems. Part 3 discusses demands nanoelectronic systems technology may make on ICCAD tools.

Presenters:

Michael Butts - Cadence Design Systems, Inc., Portland, OR

Andre DeHon - California Institute of Tech., Pasadena, CA

Seth Copen Goldstein - Carnegie Mellon Univ., Pittsburgh, PA

Time: 4:00 PM to 5:30 PM

Room: Cedar

SESSION 7A SATISFIABILITY CHECKING

Moderators: Armin Biere - ETH Zurich, Zurich, Switzerland
James H. Kukula - Synopsys, Inc., Hillsboro, OR

In recent years SAT solvers saw an incredible improvement in reasoning power. One of the most important techniques for their success is conflict driven learning. In the first paper this technique is generalized to quantified Boolean logic. The second paper applies these ideas from SAT to pseudo Boolean constraints. It also contains a comparison with ILP solvers. The final contribution of the session presents a new approach to time frame expansion for speeding up sequential verification with SAT solvers.

7A.1 CONFLICT DRIVEN LEARNING IN A QUANTIFIED BOOLEAN SATISFIABILITY SOLVER

Lintao Zhang (lintaoz@ee.princeton.edu), Sharad Malik - Princeton Univ., Princeton, NJ

7A.2 GENERIC ILP VERSUS SPECIALIZED 0-1 ILP: AN UPDATE

Fadi A. Aloul (faloul@eecs.umich.edu), Arathi Ramani, Igor Markov, Karem Sakallah - Univ. of Michigan, Ann Arbor, MI

7A.3 BINARY TIME-FRAME EXPANSION

Farzan Fallah (farzan@fla.fujitsu.com) - Fujitsu Labs. Ltd., Sunnyvale, CA

Time: 4:00 PM to 5:30 PM

Room: Pine/Fir

SESSION 7B - Videoed Session

EMERGING TECHNOLOGIES: DEVICE MODELING AND SIMULATION

Moderators: Joel R. Phillips - Cadence Berkeley Labs., San Jose, CA
Narayan R. Aluru - Univ. of Illinois, Urbana, IL

This session introduces a variety of device modeling techniques relevant for emerging technology. The first paper combines an integral formulation with precorrected-FFT techniques for simulation of biomolecule electrostatics. The second paper introduces cloud-based meshless techniques and Lagrangian approaches for efficient analysis of electrostatic MEMS. The third paper presents an approach to extract the frequency dependent inductance of structures with permeable materials.

7B.1 FAST METHODS FOR SIMULATION OF BIOMOLECULE ELECTROSTATICS

Shihhsien Kuo (skuo@mit.com), Michael D. Altman, Jaydeep P. Bardhan, Bruce Tidor, Jacob K. White - Massachusetts Institute of Tech., Cambridge, MA

7B.2 EFFICIENT MIXED-DOMAIN ANALYSIS OF ELECTROSTATIC MEMS

Gang Li, Narayan R. Aluru (aluru@uiuc.edu) - Univ. of Illinois, Urbana, IL

7B.3 FASTMAG: A 3-D MAGNETOSTATIC INDUCTANCE EXTRACTION PROGRAM FOR STRUCTURES WITH PERMEABLE MATERIALS

Yehia M. Massoud (yehia@synopsys.com) - Synopsys, Inc., Mountain View, CA
Jacob K. White - Massachusetts Institute of Tech., Cambridge, MA

Time: 4:00 PM to 5:30 PM

Room: Donner/Siskiyou

SESSION 7C CIRCUIT-LEVEL ANALOG CAD

Moderators: Rob A. Rutenbar - Carnegie Mellon Univ., Pittsburgh, PA
Henry Chang - Cadence Design Systems, Inc., San Jose, CA

This session presents new algorithms for three important phases of cell-level analog circuit design. The first paper describes the use of recently developed correlated interval arithmetic techniques—called affine arithmetic—to the problem of circuit sizing. The second paper describes a new statistical simulator for mismatch analysis. The final paper describes a new layout algorithm for analog placements with many symmetry constraints.

- 7C.1 ANALOG CIRCUIT SIZING BASED ON FORMAL METHODS USING AFFINE ARITHMETIC
Andreas Lemke (lemke@ims.uni-hannover.de), Lars Hedrich, Erich Barke - Univ. of Hanover, Hanover, Germany
- 7C.2 SISMA: A STATISTICAL SIMULATOR FOR MISMATCH ANALYSIS OF MOS ICs
Giorgio Biagetti (g.biagetti@ea.unian.it), Simone Orcioni, Loris Signoracci, Claudio Turchetti, Paolo Crippa, Michele Alessandrini - Univ. of Ancona, Ancona, Italy
- 7C.3 EFFICIENT SOLUTION SPACE EXPLORATION BASED ON SEGMENT TREES IN ANALOG PLACEMENT WITH SYMMETRY CONSTRAINTS
Florin Balasa (fbalasa@cs.uic.edu), Sarat C. Maruvada, Karthik Krishnamoorthy - Univ. of Illinois, Chicago, IL

Time: 4:00 PM to 5:30 PM

Room: Oak

SESSION 7D PHYSICAL EFFECTS IN DEEP SUB MICRON TECHNOLOGY

Moderators: Ron Duncan - Synopsys, Inc., Fremont, CA
Michel Laudes - Sun Microsystems, Inc., Sunnyvale, CA

Sub micron technology has brought with it new problems in modeling and managing parasitic effects. This session defines problems in this area, and provides novel approaches, covering noise, ESD protection, and Ebeam mask generation.

- 7D.1 POST GLOBAL ROUTING RLC CROSSTALK BUDGETING
Jinjun Xiong (jinjun@ucla.edu) - Univ. of California, Los Angeles, CA
Jun Chen, James Ma - Univ. of Wisconsin, Madison, WI
Lei He - Univ. of California, Los Angeles, CA
- 7D.2 A NEW TECHNOLOGY-INDEPENDENT CAD TOOL FOR ESD PROTECTION DEVICE EXTRACTION – ESEXTRACTOR
Rouying Zhan, Haigang Feng, Qiong Wu, Guang Chen, Albert Wang (awang@ece.iit.edu) - Illinois Institute of Tech., Chicago, IL
- 7D.3 ON MASK LAYOUT PARTITIONING FOR ELECTRON PROJECTION LITHOGRAPHY
Ruiqi Tian (ruiqi.tian@motorola.com) - Motorola, Inc. Austin, TX
Ronggang Yu - Univ. of Texas, Austin, TX
Xiaoping Tang - Cadence Design Systems, Inc., Santa Clara, CA
D. F. Wong - Univ. of Illinois, Urbana, IL

Time: 8:30 AM to 10:00 AM

Room: Cedar

SESSION 8A VERIFICATION AT THE SWITCH, GATE, AND RT LEVELS

Moderators: Ken McMillan - Cadence Berkeley Labs., Berkeley, CA
Alan Hu - Univ. of British Columbia, Vancouver, BC,
Canada

Progress continues to be made on two fundamental problems in formal verification: modeling accuracy and capacity. In this session, we see advances in switch-level model extraction, providing more accurate models with less manual intervention, and improvement in capacity based on new algorithms and abstraction.

- 8A.1 **HIGH CAPACITY AND AUTOMATIC FUNCTIONAL EXTRACTION TOOL FOR INDUSTRIAL VLSI CIRCUIT DESIGNS**
Sasha Novakovsky (nsasha@iil.intel.com), Shy Shyman, Ziyad Hanna - Intel Corp., Haifa, Israel
- 8A.2 **COMBINATIONAL EQUIVALENCE CHECKING THROUGH FUNCTION TRANSFORMATION**
Hee H. Kwak (hkwak@synopsys.com), In-Ho Moon, James H. Kukula - Synopsys, Inc., Hillsboro, OR
Thomas R. Shiple - Synopsys, Inc., Mountain View, CA
- 8A.3 **GSTE THROUGH A CASE STUDY**
Jin Yang (jin.yang@intel.com) - Intel Corp., Hillsboro, OR
Amit Goel - Carnegie Mellon Univ., Pittsburgh, PA

Time: 8:30 AM to 10:00 AM

Room: Pine/Fir

SESSION 8B NEW TRENDS IN LOGIC SYNTHESIS

Moderators: Hamid Savoj - Magma Design Automation, Inc.,
Cupertino, CA
Diana Marculescu - Carnegie Mellon Univ., Pittsburgh, PA

The first paper presents a regular PLA structure with a 4-level logic decomposition method. A new routability cost function is introduced in the second paper. The third paper discusses the flexibility in non-deterministic multi-valued networks. Finally, the last paper describes methods to synthesize reversible logic with application to quantum computation.

- 8B.1 **WHIRLPOOL PLAS: A REGULAR LOGIC STRUCTURE AND THEIR SYNTHESIS**
Fan Mo (fanmo@ic.eecs.berkeley.edu), Robert K. Brayton - Univ. of California, Berkeley, CA
- 8B.2 **BEST PAPER - METRICS FOR STRUCTURAL LOGIC SYNTHESIS**
Prabhakar Kudva (kudva@watson.ibm.com) - IBM Corp., Yorktown Heights, NY
William Dougherty, Andrew Sullivan - IBM Corp., Fishkill, NY
- 8B.3 **SIMPLIFICATION OF NON-DETERMINISTIC MULTI-VALUED NETWORKS**
Alan Mishchenko (alanmi@ee.pdx.edu) - Portland State Univ., Portland, OR
Robert K. Brayton - Univ. of California, Berkeley, CA

Time: 8:30 AM to 10:00 AM

Room: Donner/Siskiyou

**SESSION 8C MEMORY ISSUES IN
HIGH-LEVEL SYNTHESIS**

Moderators: Allen C.-H. Wu - National Tsing Hua Univ.,
Hsinchu, Taiwan, ROC
Loganath Ramachandran - Synopsys, Inc.,
Mountain View, CA

This session presents three papers addressing memory-related issues in high-level synthesis. The first paper describes a technique for synthesizing distributed memory architectures. The second paper presents an energy-aware approach for mapping data accesses to multiport memories. The last paper describes a technique for selecting addresses to minimize energy dissipation in memory arrays.

- 8C.1 **HIGH-LEVEL SYNTHESIS OF DISTRIBUTED LOGIC-MEMORY ARCHITECTURES**
Chao Huang (chaoh@ee.princeton.edu) - Princeton Univ., Princeton, NJ
Srivaths Ravi, Anand Raghunathan - NEC USA, Inc., Princeton, NJ
Niraj K. Jha - Princeton Univ., Princeton, NJ
- 8C.2 **AN ENERGY-CONSCIOUS ALGORITHM FOR MEMORY PORT ALLOCATION**
Preeti Ranjan Panda (panda@synopsys.com) - Indian Institute of Tech., New Delhi, India
Lakshmikantam Chitturi - Teradyne, Inc., San Jose, CA
- 8C.3 **ENERGY EFFICIENT ADDRESS ASSIGNMENT THROUGH MINIMIZED MEMORY ROW SWITCHING**
Sambuddhi Hettiaratchi (s.hetti@ic.ac.uk), Peter Y. Cheung, Thomas J. Clarke - Imperial College, London, UK

Time: 8:30 AM to 10:00 AM

Room: Oak

**SESSION 8D NOISE EFFECTS
ON CIRCUIT OPERATION**

Moderators: Florentin Dartu - Intel Corp., Hillsboro, OR
Anirudh Devgan - IBM Corp., Austin, TX

This session presents new advances in the critical area of noise and its impact on circuit performance and functionality. The first paper refines timing analysis to be suitable for capturing noise effects. The second paper improves upon noise propagation and failure criteria and the last paper will describe an efficient circuit reduction technique for crosstalk estimation.

- 8D.1 **REFINING SWITCHING WINDOW BY TIME SLOTS FOR CROSSTALK NOISE CALCULATION**
Pinhong Chen (pinhong@eecs.berkeley.edu) - Univ. of California, Berkeley, CA
Yuji Kukimoto - Cadence Design Systems, Inc., San Jose, CA
Kurt Keutzer - Univ. of California, Berkeley, CA
- 8D.2 **NOISE PROPAGATION AND FAILURE CRITERIA FOR VLSI DESIGNS**
Vladimir Zolotov - Motorola, Inc., Austin, TX
David Blaauw (blaauw@umich.edu) - Univ. of Michigan, Ann Arbor, MI
Supamas Sirichotiyakul - Sun Microsystems, Boston, MA
Murat Becer, Chanhee Oh, Rajendran Panda - Motorola, Inc., Austin, TX
Amir Grinshpon, Rafi Levy - Motorola, Inc., Austin, TX
- 8D.3 **EFFICIENT CROSSTALK NOISE MODELING USING AGGRESSOR AND TREE REDUCTION**
Li Ding (lding@eecs.umich.edu), David Blaauw,

Time: 10:30 AM to 12:00 PM

Room: Cedar

SESSION 9A LOW LEVEL AWARE BEHAVIORAL SYNTHESIS

Moderators: Forrest D. Brewer - Univ. of California,
Santa Barbara, CA
Barry Pangrle - Synopsys, Inc., Mountain View, CA

In this session, quality metrics associated with design issues at lower abstraction levels augment behavioral synthesis techniques to improve the quality of results. The first paper describes a decomposition technique to address heterogeneous word widths and bit level scheduling. In the second paper, power issues in the interconnections are used to optimize the total power dissipation. In the final paper, resource sharing is examined in the context of floorplanning issues in a combined algorithm.

9A.1 BIT-LEVEL SCHEDULING OF HETEROGENEOUS BEHAVIORAL SPECIFICATIONS

Maria C. Molina (cmolinap@dacya.ucm.es),
Jose M. Mendias, Roman Hermida -
Complutense Univ., Madrid, Spain

9A.2 COUPLING-AWARE HIGH-LEVEL INTERCONNECT SYNTHESIS FOR LOW POWER

Chun-Gi Lyuh, Taewhan Kim (tkim@cs.kaist.ac.kr) -
KAIST, Taejon, Korea
Kiwook Kim - Pluris Inc., Cupertino, CA

9A.3 LAYOUT-DRIVEN RESOURCE SHARING IN HIGH-LEVEL SYNTHESIS

Junhyung Um, Jaehoon Kim, Taewhan Kim
(tkim@cs.kaist.ac.kr) - KAIST, Taejon, Korea

Time: 10:30 AM to 12:00 PM

Room: Pine/Fir

SESSION 9B ADVANCES IN TIMING ANALYSIS ACCURACY

Moderators: Tim Burks - Magma Design Automation, Inc.,
Cupertino, CA
David Blaauw - Univ. of Michigan, Ann Arbor, MI

Accurate timing analysis is more important than ever before. These papers provide three ways to increase accuracy. The first two papers present advances in delay computation methods. The third paper shows how to avoid excessive pessimism in timing analysis that includes on-chip delay variation.

9B.1 A DELAY METRIC FOR RC CIRCUITS BASED ON THE WEIBULL DISTRIBUTION

Frank Liu (frankliu@us.ibm.com), Chandramouli Kashyap,
Charles J. Alpert - IBM Corp., Austin, TX

9B.2 WTA - WAVEFORM-BASED TIMING ANALYSIS FOR DEEP SUBMICRON CIRCUITS

Larry McMurchie (larry@ee.washington.edu), Carl Sechen -
Univ. of Washington, Seattle, WA

9B.3 GENERAL FRAMEWORK FOR REMOVAL OF CLOCK NETWORK PESSIMISM

Jindrich Zejda (zejdaj@synopsys.com) - Synopsys, Inc.,
Mountain View, CA
Paul Frain - Synopsys, Inc., Dublin, Ireland

Time: 10:30 AM to 12:30 PM

Room: Donner/Siskiyou

**SESSION 9C CUSTOMIZATION OF
EMBEDDED SYSTEM ARCHITECTURES**

Moderators: Petru Eles - Linköping Univ., Linköping, Sweden
Hiroyuki Tomiyama - ISIT, Fukuoka, Japan

Customizing the architecture of an embedded system can yield excellent performance and power benefits. The first two papers in this session describe automated techniques for creating a customized instruction set for an application-specific instruction-set processor. The third paper introduces fast exploration methods to generate a customized low-power loop cache. The fourth paper discusses a modeling framework to support creation of custom on-chip bus architectures.

- 9C.1 **SYNTHESIS OF CUSTOM PROCESSORS
BASED ON EXTENSIBLE PLATFORMS**
Fei Sun (fsun@ee.princeton.edu) - Princeton Univ., Princeton, NJ
Srivaths Ravi, Anand Raghunathan - NEC USA, Inc., Princeton, NJ
Niraj K. Jha - Princeton Univ., Princeton, NJ
- 9C.2 **EFFICIENT INSTRUCTION ENCODING FOR AUTOMATIC
INSTRUCTION SET DESIGN OF CONFIGURABLE ASIPS**
Jong-eun Lee (jelee@poppy.snu.ac.kr), Kiyoungh Choi -
Seoul National Univ., Seoul, Korea
Nikil Dutt - Univ. of California, Irvine, CA
- 9C.3 **SYNTHESIS OF CUSTOMIZED LOOP CACHES
FOR CORE-BASED EMBEDDED SYSTEMS**
Susan Cotterell (susanc@cs.ucr.edu), Frank Vahid -
Univ. of California, Riverside, CA
- 9C.4 **A HIERARCHICAL MODELING FRAMEWORK FOR
ON-CHIP COMMUNICATION ARCHITECTURES**
Xinping Zhu (xzhu@ee.princeton.edu), Sharad Malik -
Princeton Univ., Princeton, NJ

Time: 10:30 AM to 12:30 PM

Room: Oak

**SESSION 9D ADVANCES
IN COMBINATIONAL SYNTHESIS**

Moderators: Olivier Coudert - Monterey Design Systems,
Sunnyvale, CA
Prabhakar Kudva - IBM Corp., Yorktown Heights, NY

This session presents new ideas in combinational synthesis. The first paper addresses SPFD rewiring for improving rewiring ability. The second paper proposes one optimization method based on information flows. Symbolic Boolean decomposition is addressed in the next paper. Finally, the last paper proposes logic function folding for LUT area optimization.

- 9D.1 **A NEW ENHANCED SPFD REWIRING ALGORITHM**
Jason Cong, Joey Y. Lin (yizhou@cs.ucla.edu) -
Univ. of California, Los Angeles, CA
Wangning Long - Aplus Design Tech., Inc., Los Angeles, CA
- 9D.2 **TOPOLOGICALLY CONSTRAINED LOGIC SYNTHESIS**
Subarnarekha Sinha (subarna@eecs.berkeley.edu) -
Univ. of California, Berkeley, CA
Alan Mishchenko - Portland State Univ., Portland, OR
Robert K. Brayton - Univ. of California, Berkeley, CA
- 9D.3 **RESYNTHESIS OF MULTI-LEVEL CIRCUITS UNDER TIGHT
CONSTRAINTS USING SYMBOLIC OPTIMIZATION**
Victor N. Kravets (kravets@us.ibm.com) - IBM Corp., Yorktown
Heights, NY
Karem A. Sakallah - Univ. of Michigan, Ann Arbor, MI
- 9D.4 **FOLDING OF LOGIC FUNCTIONS AND ITS APPLICATION TO LOOK
UP TABLE COMPACTION**
Shinji Kimura (shinji_kimura@waseda.jp), Takashi Horiyama -
Waseda Univ., Kitakyushu, Japan
Masaki Nakanishi, Hirotsugu Kajihara - Nara Institute of
Science & Tech., Ikoma, Japan

Time: 2:00 PM to 3:30 PM

Room: Cedar

SESSION 10A SYSTEM-LEVEL PERFORMANCE AND POWER MODELING AND OPTIMIZATION

Moderators: Frank Vahid - Univ. of California, Riverside, CA
Xiaobo (Sharon) Hu - Univ. of Notre Dame, Notre Dame, IN

Performance and power modeling is an essential step towards designing efficient electronic systems. The first paper in this session presents an approach to performance estimation of multiprocessor real-time systems, based on stochastic models. The second paper is dealing with the issue of power management for battery-driven systems. The third paper handles leakage power reduction at system level using power and timing models derived from detailed circuit designs.

10A.1 SCHEDULABILITY ANALYSIS OF MULTIPROCESSOR REAL-TIME APPLICATIONS WITH STOCHASTIC TASK EXECUTION TIMES

Sorin Manolache (sorma@ida.liu.se), Petru Eles, Zebo Peng -
Linköping Univ., Linköping, Sweden

10A.2 BATTERY-AWARE POWER MANAGEMENT BASED ON MARKOVIAN DECISION PROCESSES

Peng Rong (prong@usc.edu), Massoud Pedram -
Univ. of Southern California, Los Angeles, CA

10A.3 LEAKAGE POWER MODELING AND REDUCTION WITH DATA RETENTION

Weiping Liao - Univ. of California, Los Angeles, CA
Joseph M. Basile - Intel Corp., Santa Clara, CA
Lei He (lhe@ee.ucla.edu) - Univ. of California,
Los Angeles, CA

Time: 2:00 PM to 3:30 PM

Room: Pine/Fir

SESSION 10B ADVANCES IN DYNAMIC VOLTAGE SCHEDULING

Moderators: Rajesh K. Gupta - Univ. of California, Irvine, CA
Miodrag Potkonjak - Univ. of California, Los Angeles, CA

The papers in this session address advances in Dynamic Voltage Scheduling and their use in applications. The first paper provides an analytical model combining Dynamic Voltage Scaling and Body Biasing in an attempt to optimize power in microprocessor blocks. The second paper considers the overhead during voltage transition in DVS to minimize overall power. The final paper presents a detailed case analysis of an MPEG decoder that can benefit from Dynamic Voltage Scaling.

10B.1 COMBINED DYNAMIC VOLTAGE SCALING AND ADAPTIVE BODY BIASING FOR LOWER POWER MICROPROCESSORS UNDER DYNAMIC WORKLOADS

Steven M. Martin (stevenmm@umich.edu),
Krisztian Flautner, Trevor Mudge, David Blaauw -
Univ. of Michigan, Ann Arbor, MI

10B.2 A REALISTIC VARIABLE VOLTAGE SCHEDULING MODEL FOR REAL-TIME APPLICATIONS

Bren C. Mochocki (bmochock@cse.nd.edu),
Xiaobo (Sharon) Hu - Univ. of Notre Dame, Notre Dame, IN

10B.3 FRAME-BASED DYNAMIC VOLTAGE AND FREQUENCY SCALING FOR A MPEG DECODER

Ki Hwan Choi (kihwanchoi@usc.edu), Karthik Dantu,
Wei Chung Cheng, Massoud Pedram -
Univ. of Southern California, Los Angeles, CA

Time: 2:00 PM to 3:30 PM

Room: Donner/Siskiyou

SESSION 10C TECHNIQUES IN PLACEMENT

Moderators: Lukas P.P. van Ginneken - Magma Design Automation, Inc., Cupertino, CA
Kia Bazargan - Univ. of Minnesota, Minneapolis, MN

This session presents new techniques related to placement, including Rent's rule based on congestion minimization, free space management for partition-based placement, and incremental placement for FPGAs.

- 10C.1 CONGESTION MINIMIZATION DURING PLACEMENT WITHOUT ESTIMATION
Bo Hu (hb@ece.ucsb.edu), Malgorzata Marek-Sadowska - Univ. of California, Santa Barbara, CA
- 10C.2 FREE SPACE MANAGEMENT FOR CUT-BASED PLACEMENT
Charles J. Alpert, Gi-Joon Nam (gnam@us.ibm.com), Paul Villarrubia - IBM Corp., Austin, TX
- 10C.3 INCREMENTAL PLACEMENT FOR LAYOUT-DRIVEN OPTIMIZATIONS ON FPGAS
Deshanand P. Singh (singhd@eecg.toronto.edu), Stephen D. Brown - Univ. of Toronto, Toronto, ON, Canada

Time: 2:00 PM to 3:30 PM

Room: Oak

SESSION 10D MODEL ORDER REDUCTION

Moderators: Mustafa Celik - Magma Design Automation, Inc., Cupertino, CA
Sharad Kapur - Agere Systems, Inc., Murray Hill, NJ

This session includes three order reduction papers. The first paper presents SNOR, an order reduction method for circuits containing susceptance elements. The second paper proposes a new multi-node explicit moment-matching method. The session concludes with a passive constrained fitting algorithm for measured frequency-domain data.

- 10D.1 ROBUST AND PASSIVE MODEL ORDER REDUCTION FOR CIRCUITS CONTAINING SUSCEPTANCE ELEMENTS
Hui Zheng (hzheng@ece.cmu.edu), Lawrence T. Pileggi - Carnegie Mellon Univ., Pittsburgh, PA
- 10D.2 EFFICIENT MODEL ORDER REDUCTION VIA MULTI-NODE MOMENT MATCHING
Yehea I. Ismail (ismail@ece.northwestern.edu) - Northwestern Univ., Evanston, IL
- 10D.3 OPTIMIZATION BASED PASSIVE CONSTRAINED FITTING
Carlos P. Coelho - INESC, Lisboa, Portugal
Joel R. Phillips - Cadence Berkeley Labs., San Jose, CA
Luis Miguel Silveira (lms@inesc-id.pt) - INESC, Lisboa, Portugal

Wednesday, November 13, 2002

ICCAD-2002

Time: 4:00 PM to 5:30 PM

Room: Pine/Fir between using SAT and BDDs for sequential property checking.

SESSION 11A EMBEDDED TUTORIAL: SAT & ATPG: BOOLEAN ENGINES FOR
FORMAL HARDWARE VERIFICATION

Moderators: Joao Marques-Silva - Tech. Univ. Lisbon, Lisboa, Portugal
Karem A. Sakallah - Univ. of Michigan, Ann Arbor, MI

Even after years of research, algorithms for Boolean decision making have remained a hot field of research. Progress in SAT and ATPG has led to a new generation of logic synthesis and verification techniques with high impact in industrial practice. SAT and ATPG are closely related problems. They are not only based on similar algorithmic concepts, they also play a similar role in many applications of electronic design automation. Historically, however, SAT and ATPG have developed quite independently with limited interaction. While research in ATPG was primarily driven by applications in circuit testing, SAT evolved from a more general computer science background.

In this tutorial, we briefly review the basic notions of SAT and ATPG and highlight the common themes as well as differences. We discuss the pros and cons of representing circuits as multi-level netlists as in ATPG (or structural SAT) as opposed to CNF representations as in SAT. We elaborate on this by studying two important applications of SAT and ATPG. We consider formal verification where SAT formulations are more popular and logic synthesis where ATPG provides a more general framework of reasoning.

Equivalence checking of circuits is the most successful formal verification technique in industry. As a pure combinational problem, equivalence checking can naturally be described as a SAT problem.

We discuss how SAT techniques can make equivalence checking more robust and why these techniques have not been used in the first place. The next challenge in formal methods is checking of sequential properties, also known as model checking. With the idea of bounded model checking it became possible to use sophisticated SAT and ATPG implementations to check sequential designs. This approach is usually not complete but much more robust. We will also discuss tradeoffs

Logic synthesis is a process which optimizes design implementation towards a specific goal, such as better area, power, and performance. ATPG provides a reasoning engine to search for good logic restructuring opportunities in an extremely efficient fashion. The fast runtime and low memory usage make it the candidate-of-choice for many industrial-strength logic synthesis tools. In this tutorial, we will introduce the concept of rewiring - the ATPG-based logic restructuring technique to manipulate interconnections in a gate-level netlist. Rewiring is a general form of the traditional Boolean factorization, but can be done much more efficiently. We will review relevant ATPG techniques in logic synthesis and their applications to post-layout logic restructuring for design closure.

Presenters:

Wolfgang Kunz - Univ. of Kaiserslautern,
Kaiserslautern, Germany
Armin Biere - ETH Zurich, Zurich, Switzerland
Malgorzata Marek-Sadowska - Univ. of California,
Santa Barbara, CA
Chih-Wei (Jim) Chang - Cadence Design Systems, Inc.,
San Jose, CA

Time: 4:00 PM to 5:30 PM

Room: Donner/Siskiyou

SESSION 11B EMBEDDED TUTORIAL: THE A TO Z OF SoCs

Moderators: Grant E. Martin - Cadence Berkeley Labs., Berkeley, CA
Kees A. Vissers - Chameleon Systems, Inc., San Jose, CA

The exploding complexity of new chips and the ever decreasing time-to-market window are forcing fundamental changes in the way systems are designed. The advent of Systems-on-Chip (SoC) based on pre-designed intellectual-property (IP) cores has become an absolute necessity for embedded systems companies to remain competitive. Designing an SoC, however, is extremely complex, as it encompasses a range of difficult problems in hardware and software design. On the hardware side, an SoC can be seen as a very large application specific integrated circuit (ASIC) comprising complex cores, memory blocks, custom logic and mixed-signal circuits. This combination of diverse blocks in a very large chip transforms the usual problems of synthesis, timing and layout (found in ASIC design) into significantly more complex issues of synthesis capacity, timing correction, wireability, power, etc. Moreover, there are significant challenges in integrating diverse components such as mixed-signal, digital and memory blocks.

On the software side, designing an SoC requires careful analysis of the application software requirements, coupled with the characteristics of the real-time operating system and the hardware-software interface (device drivers). The tight interaction of hardware and software in SoCs causes unique design and verification problems which demand specialized methodology, tools and techniques.

This presentation will cover a wide range of SoC issues including market drivers and trends, technology and integration aspects, early architecture definition, methodology, hardware and software design and verification techniques. Among the topics covered are:

Technical and market issues that lead to the development of system-on-chip technologies; problems in integrating diverse technologies such as mixed-signal, memories and digital components; future trends and roadblocks for SoCs, including systems-on-a-package; current approaches for SoC design using cores and platforms; SoC design methodology; architectural design issues; performance analysis of SoCs; hardware design; and embedded software design-verification issues.

Presenters:

Reinaldo Bergamaschi - IBM Corp., Yorktown Heights, NY
John Cohn - IBM Microelectronics, Essex Junction, VT

Tutorials9:00 AM - 5:00 PM

Registration8:00 AM - 10:00 AM

Tutorial 1 - High Performance Integrated Circuit Analysis and Design Including On-Chip Inductance

Cedar Ballroom

Speakers: Chandramouli Kashyap - IBM Corp., Austin TX
Byron Krauter - IBM Corp., Austin, TX
Yehea I. Ismail - Northwestern Univ., Chicago, IL
Sachin Sapatnekar - Univ. of Minnesota, Minneapolis, MN

Background: On-chip inductance significantly affects the performance of chips in current technologies. These effects are expected to increase in future technologies due to several technology trends. Some of these trends are the exponentially increasing operating frequencies, lower resistivity interconnect (such as copper), low K dielectrics, faster devices (such as SOI and SiGe technologies), improved cooling techniques, and wider busses. The target audience consists of circuit designers, CAD engineers, and academic researchers. Familiarity with basic concepts in circuit design, model order reduction, extraction techniques, and design methodologies is assumed.

Description: The first part of the tutorial discusses the growing importance of on-chip inductance and its effects on propagation delay, rise time, power consumption, and noise. These effects are discussed both quantitatively and intuitively. This part also characterizes how important inductance effects are in current technologies.

The second part discusses the problem of inductance extraction. 3D full extraction techniques are discussed. Other techniques with lower computational complexity are also discussed such as 2-D and 2-D

extraction techniques and analytical approximate methods. The problem of determining the return paths is also discussed for these approximate techniques. The sensitivity of delay and performance estimations to errors in extracted inductance values is also discussed.

The third part discusses noise and inductive coupling effects. Wide busses are of specific interest. Model order reduction techniques that can efficiently handle multi-input circuits with large amount of coupling are also discussed. Realizable reduced order models are presented for RLC circuits.

The fourth part discusses design methodologies including inductance. Physical design and timing of integrated circuits including inductance is presented. The effects of inductance on repeater insertion, impedance matching, and wire and transistor sizing are discussed.

The fifth part discusses inductance effects in global distribution networks such as clock and power distribution networks.

Finally, future trends and expectations for inductance effects with technology scaling are discussed in the sixth part.

Tutorials9:00 AM - 5:00 PM

Registration8:00 AM - 10:00 AM

Tutorial 2 - FPGAs: Computer-Aided Design, Applications and Future Architectures

Pine Ballroom

Speakers: Jeffrey Arnold - Stretch, Inc., Los Gatos, CA
 Kia Bazargan - Univ. of Minnesota, Minneapolis, MN
 Maya Gokhaleh - Los Alamos National Lab., Los Alamos, NM
 Mark Jones - Virginia Tech., Blacksburg, VA
 Alireza Kaviani - Xilinx, Inc., San Jose, CA

Background: With increasing system complexities and the need to reduce manufacturing costs, use of FPGAs in SOC designs is becoming inevitable. An FPGA component in SOC would increase fault tolerance and product durability, because the FPGA fabric can be tailor-made in the running environment of the system with new configurations to either overcome faults or reflect updates to the original design. This tutorial addresses issues that facilitate utilizing FPGAs in such a context. The target audience consists of circuit designers, CAD engineers and academic researchers.

Description: The first part of the tutorial covers existing and emerging commercial and academic FPGA architectures. We discuss the effects of different architectural options such as the granularity of functional units on the FPGA, size and physical distribution of memory modules within the FPGA fabric, embedding the FPGA fabric within an ASIC design or vice-versa, hierarchical structures and communication mechanisms for inter- and intra-FPGA data transfers.

The second part describes computer aided design methods for FPGAs, including synthesis, technology mapping, and physical design.

Different design effort / quality requirements at the development and the final optimization phases call for approaches that provide trade-offs between short design cycles and high clock frequencies. Higher quality expectations require interaction between synthesis and physical design. We also address the need for incremental design flows. Finally, we will address physical design algorithms that facilitate runtime reconfiguration of the FPGA fabric.

The third part surveys current C-to-hardware methods, including languages, compilation and high-level synthesis. Such methods are necessary for fast HW/SW co-design of large SOC designs. Memory block allocation in the FPGA fabric and resource allocation / scheduling will be discussed.

The fourth part will survey FPGA and reconfigurable computing applications that have shown significant improvements over ASIC implementations in terms of speed, power consumption and size. The present state and the future of dynamically reconfigurable systems will be discussed.

Tutorials9:00 AM - 5:00 PM

Registration8:00 AM - 10:00 AM

Tutorial 3 - Specification and Design of Multimillion Gate SOCs

Fir Ballroom

Speakers: Ramesh Chandra - ST Microelectronics, San Diego, CA
Joerg Henkel - NEC USA, Inc., Princeton, NJ
Preeti Ranjan Panda - Indian Institute of Tech., New Delhi, India
Sridevan Parameswaran - Univ. of New South Wales, New South Wales, Australia
Loganath Ramachandran - Synopsys, Inc., Mountain View, CA

Background: Advances in technology have made it possible to integrate several multi-million transistors on a single chip. However, design and verification teams face several challenges not been seen before: modeling and verifying entire system functionality, closing early on the system level architecture, extensive simulations of the hardware and software components and the final path to implementation of the entire SOC. New specification languages, new modeling and design paradigms, and new verification methods are evolving to meet these challenges.

Description: This tutorial will cover the state-of-the-art in specification and design methodologies. It will benefit design engineers, managers, researchers and students who are interested in understanding these new modeling, design and verification paradigms. This full-day tutorial is structured into five major parts.

- (a) System level design challenges from a designer's perspective
- (b) Specification languages for system level design
- (c) Functional and architectural modeling and verification
- (d) Platform based design concepts
- (e) Path from specification to implementation

An overview of the real challenges faced by system level designers will be presented with examples. The weaknesses of traditional design methods will be highlighted, thereby motivating the need for newer system level design tools and methodologies.

Several modeling languages that focus on system level have been proposed in the recent years. Languages such as SystemC, SpecC, and Superlog represent different approaches for specifying the entire system. In this section of the tutorial, we will present an overview of

these approaches, explain the specific properties of these languages and discuss in detail the application of various system modeling principles in SystemC.

In the next section of the tutorial we will focus on system level verification, which includes both functional and architectural verification. Functional verification addresses the modeling of the entire system functionality in order to understand system level performance issues. In general this requires heterogeneous modeling involving several models of computation. Architectural verification addresses architectural tradeoff issues that enable designers to close on the architecture early in the design cycle. This is achieved using transaction level models (TLMs) of the system components.

One popular method to manage SOC design complexity is to define a platform, which is an abstraction that embodies the lower level details. Such a platform along with an associated RTOS, forms the backbone for the SOC design. The next part of the tutorial will deal with the underlying concepts of platform-based design methodologies and their advantages compared to traditional system design concepts. Examples of commercial platforms will be presented.

The path to implementation from system level specification can be in any one of three domains: software; hardware; or hardware/software. In the software realization path, we will present modern compiler tools and techniques specifically targeted towards application specific systems. In the hardware section, we will present techniques for synthesis and discuss quality of results for designs created from system level specifications. Finally in the hardware/software implementation we will show the procedures that can lead to single/multi processor systems and ASIPs.

Tutorials9:00 AM - 5:00 PM

Registration8:00 AM - 10:00 AM

Tutorial 4 - Placement - the Key Problem in Physical Design

Oak Ballroom

Speakers: Jürgen Koehl - IBM Microelectronics, Essex Junction, VT
 John Lillis - Univ. of Illinois, Chicago, IL
 Salil Rajee - Hierarchical Design Inc., Santa Clara, CA
 Jens Vygen - Univ. of Bonn, Bonn, Germany

Background: Placement is one of the main tasks in physical layout. The quality of the placement becomes more and more important with shrinking feature sizes for several reasons: routability is harder to achieve; the wireload has an increasing impact on the timing behavior; and minimizing power consumption (which depends on the overall wire capacitance, and thus on the placement) is an increasingly important objective. However, even for the classical (and still useful) problem formulations, many questions have remained open. An additional challenge is posed by increasing complexities of chips, where placement has to deal with several million movable components.

The target audience includes design engineers, academic researchers, and anyone interested in physical design.

Description: This tutorial starts with a description of an automated design flow from a designer's viewpoint. The design objectives are discussed, and the key role of the placement problem, in interaction with other tasks like routing, timing optimization, logic changes and clocktree design, is stressed. Examples of current production parts and future trends highlight the design complexities that need to be supported. The first part ends with addressing the question of hierarchical versus flat design and illuminating some pros and cons.

The second part discusses hierarchy, and, in particular, floorplanning. We will discuss the two approaches to hierarchical physical implementation: one, the top-down floorplanning approach and two, the bottom-up partitioning approach. Key technologies that enable both approaches will be enumerated. We will discuss a few floorplan

representations and talk about algorithms used by current block placers. We will also talk about pin assignment techniques, and timing budgeting for hierarchical implementation.

Basic placement algorithms are subject of the third part of this tutorial. Classical formulations of the placement problem, though still useful, are far from being well-solved in spite of intensive research for decades. We will summarize what is known in theory, review the most successful placement approaches, and discuss their pros and cons. Stability and robustness is essential for achieving design closure when integrating other tools (like timing optimization) and objectives into the placement flow. While the classical and most common objective in global placement is minimization of some weighted netlength estimation, the goal in detailed placement (legalization) is usually rather to minimize the weighted total movement. We discuss both problems, their objectives, constraints, and solution techniques in theory and practice.

The effects of placement on the timing and routability properties of a circuit are paramount. The fourth part of this tutorial will give an overview of the state of knowledge in this area and will discuss potential future directions. Timing related topics will include performance models, path-based versus net-based timing optimization and implications of post-placement optimizations such as buffer insertion. In the routability area, congestion modeling and validation including constructive versus statistical models will be discussed. A discussion of global and detailed routability optimization techniques is also planned.