

GENERAL INFORMATION

SUNDAY **NOVEMBER 5, 2000**

Early Registration (Bayshore Foyer)	5:00 PM - 8:00 PM
ACM/SIGDA Meeting (Donner Room)	5:30 PM - 8:30 PM

MONDAY **NOVEMBER 6, 2000** **Page 18**

Registration (Bayshore Foyer)	7:30 AM - 5:00 PM
Continental Breakfast (Sierra/Cascade Ballroom)	8:00 AM - 9:00 AM
Speakers' Breakfast (Monterey Room)	8:00 AM - 9:00 AM
Opening Session Keynote Address (Gateway Ballroom)	9:00 AM - 10:15 AM
Lunch (Sierra/Cascade Ballroom)	12:30 PM - 2:00 PM

TUESDAY **NOVEMBER 7, 2000** **Page 28**

Registration (Bayshore Foyer)	7:30 AM - 5:00 PM
Continental Breakfast (Sierra/Cascade Ballroom)	8:00 AM - 9:00 AM
Speakers' Breakfast (Monterey Room)	8:00 AM - 9:00 AM
Lunch (Sierra/Cascade Ballroom)	12:30 PM - 2:00 PM
Panel: Why Doesn't EDA Get Enough Respect? (Gateway Ballroom)	4:00 PM - 5:30 PM
Cocktail Reception (Sierra/Cascade Ballroom)	5:30 PM - 7:00 PM

WEDNESDAY **NOVEMBER 8, 2000** **Page 44**

Registration (Bayshore Foyer)	8:00 AM - 5:00 PM
Continental Breakfast (Sierra/Cascade Ballroom)	8:00 AM - 9:00 AM
Speakers' Breakfast (Monterey Room)	8:00 AM - 9:00 AM
Lunch (Sierra/Cascade Ballroom)	12:30 PM - 2:00 PM

THURSDAY **NOVEMBER 9, 2000** **Page 58**

Continental Breakfast (Gateway Foyer)	8:00 AM - 9:00 AM
Tutorial Registration (Bayshore Foyer)	8:00 AM - 10:00 AM
Lunch (Gateway Foyer)	12:00 PM - 1:00 PM

Vendor Suites open, by invitation only, November 6, 7, & 8.


ICCAD-2000 AT A GLANCE

SUNDAY, NOVEMBER 5

Early Registration, 5:00PM - 8:00PM - (Bayshore Foyer)
ACM/SIGDA Meeting, 5:30PM - (Donner Room)

MONDAY, NOVEMBER 6


Continental Breakfast - 8:00 AM (Sierra/Cascade Ballroom)
Speakers' Breakfast - 8:00 AM (Monterey Room)
Vendor Suites - Open by Invitation

 Opening Session/Keynote Address
LET'S GET PHYSICAL : ASIC/SOC DESIGN IN THE ERA OF WIRE - LIMITED TECHNOLOGY
William J. Dally
Professor, Stanford Univ.
Chief Technical Officer, Chip2Chip, Inc.
(Gateway Ballroom)

Coffee Break provided by:
Cadabra Design, A Numerical Company

Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom
1A Floorplanning and Partitioning	1B High Level Simulation	1C Methods for DSP Synthesis and Debugging	1D Issues in Timing Estimation

Lunch
(Sierra/Cascade Ballroom)

 2A Embedded Tutorial: Communication Designs: System Synthesis Challenges and Opportunities (Pine/Fir Ballroom)	2B Embedded Tutorial: Challenges in Physical Chip Design (Donner/Siskiyou Ballroom)
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Coffee Break provided by:
Cadabra Design, A Numerical Company

Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom
3A Topics in Routing	3B Partial Verification Techniques	3C Scheduling and Compilation for Embedded Systems	3D Inductance and Full Wave Analysis

ICCAD-2000 AT A GLANCE

TUESDAY, NOVEMBER 7


Continental Breakfast - 8:00 AM (Sierra/Cascade Ballroom)
Speakers' Breakfast - 8:00 AM (Monterey Room)
Vendor Suites - Open by Invitation

Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom
4A Placement I	4B High-Level Design Tools for Analog Circuits	4C Delay Budgeting and Distribution	 4D Interconnect Analysis


Coffee Break provided by:
Cadabra Design, A Numerical Company

5A Embedded Tutorial: Incremental CAD (Pine/Fir Ballroom)	5B Embedded Tutorial: Decomposing Model Checking Tasks Using the Assume-Guarantee Paradigm (Donner/Siskiyou Ballroom)
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Lunch
(Sierra/Cascade Ballroom)

Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom
6A Placement II	6B Analog and RF Simulation	6C Markovian Analysis and Asynchronous Circuits	 6D Low Power Interconnect Modeling and Optimization

Coffee Break provided by:
Magma Design Automation

 7A
PANEL:
WHY DOESN'T EDA GET ENOUGH RESPECT?
(Gateway Ballroom)

COCKTAIL RECEPTION
5:30PM - 7:00PM
(SIERRA / CASCADE BALLROOM)

ICCAD-2000 AT A GLANCE

WEDNESDAY, NOVEMBER 8

Continental Breakfast - 8:00 AM (Sierra/Cascade Ballroom)
 Speakers' Breakfast - 8:00 AM (Monterey Room)
 Vendor Suites - Open by Invitation

Cedar Ballroom	Pine/Fir Ballroom	Donner/Siskiyou Ballroom	Oak Ballroom
8A Static Timing Analysis	8B Embedded Systems Power Management and Validation	8C Advances in Layout and Synthesis	8D Embedded Tutorial: Test of Future SoC

Coffee Break

9A Noise and Performance Issues in Routing	9B Communication Architectures Design and Analysis	9C Performance Driven Logic Synthesis	9D New Approaches to At-Speed BIST and Diagnosis
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Lunch
 (Sierra/Cascade Ballroom)

10A Power Analysis and Optimization	10B VLIW Exploration and Design Synthesis	10C Flexibility in Logic Synthesis	10D Digital and Analog Test Generation
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Coffee Break

11A Embedded Tutorial: System and Architecture-Level Power Reduction for Microprocessor-Based Communication and Multi-Media Applications <i>(Donner/Siskiyou Ballroom)</i>	11B Embedded Tutorial: Design-Manufacturing Interface for 0.13 Micron and Below <i>(Pine/Fir Ballroom)</i>
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Mark your calendar

ICCAD-2001, November 4 - 8

ICCAD-2000 AT A GLANCE

FULL-DAY TUTORIALS

Continental Breakfast - 8:00AM - 9:00AM (Gateway Foyer)
 Tutorial Registration - 8:00AM - 10:00AM (Bayshore Foyer)
 Lunch - 12:00PM - 1:00PM (Gateway Foyer)

THURSDAY, NOVEMBER 9

9:00 AM TUTORIAL 1 5:00 PM

Modern Physical Design: Algorithm Technology and Methodology

(CEDAR BALLROOM)

9:00 AM TUTORIAL 2 5:00 PM

Interconnect-Centric Design and Analysis for Electrical Integrity in Systems-on-a-Chip

(PINE BALLROOM)

9:00 AM TUTORIAL 3 5:00 PM

Symbolic Model Checking: Principles and Advanced Techniques

(FIR BALLROOM)

9:00 AM TUTORIAL 4 5:00 PM

Gain-Based Logic Synthesis

(OAK BALLROOM)

Time: 11:00 AM to 12:30 PM

Room: Cedar

FLOORPLANNING AND PARTITIONING

Moderators: *Charles J. Alpert* - IBM Corp., Austin, TX
Carl Sechen - Univ. of Washington, Seattle, WA

This session covers topics in floorplanning and partitioning. The first paper presents a top-down approach to partitioning and floorplanning with retiming. The next two papers present fundamentally new representations for non-slicing floorplans. The final paper presents a study of the performance of incremental optimization tools for partitioning, placement, and routing.

1A.1 A NOVEL APPROACH TO PHYSICAL PLANNING WITH RETIMING

Jason Cong (*cong@cs.ucla.edu*), *Sung Kyu Lim* - Univ. of California, Los Angeles, CA

1A.2 CORNER BLOCK LIST: AN EFFECTIVE AND EFFICIENT TOPOLOGICAL REPRESENTATION OF NON-SLICING FLOORPLAN

Xianlong Hong, *Gang Huang*, *Yici Cai*, *Jiangchun Gu*, *Sheqin Dong* - Tsinghua Univ., Beijing, China
Chung-Kuan Cheng (*kuan@cs.ucsd.edu*) - Univ. of California at San Diego, La Jolla, CA
Jun Gu - Univ. of Hong Kong, Hong Kong, China

1A.3 MODELING NON-SLICING FLOORPLANS WITH BINARY TREES

Florin Balasa (*fbalasa@eecs.uic.edu*) - Univ. of Illinois, Chicago, IL

1A.4 SON MISMATCHES BETWEEN INCREMENTAL OPTIMIZERS AND INSTANCE PERTURBATIONS IN PHYSICAL DESIGN TOOLS

Andrew B. Kahng, *Stefanus Mantik* (*stefanus@cs.ucla.edu*) - Univ. of California, Los Angeles, CA

Time: 11:00 AM to 12:30 PM

Room: Pine/Fir

HIGH LEVEL SIMULATION

Moderators: *James H. Kukula* - Synopsys, Inc., Beaverton, OR
Vigyan Singhal - Tempus Fugit, Inc., Fremont, CA

Simulation is still the dominant method for validating designs. This session presents contributions to three disparate aspects of simulation and accelerating simulator code, measuring coverage of embedded software simulation, and automatically generating test benches for memory access protocols.

1B.1 EVENT DRIVEN SIMULATION WITHOUT LOOPS OR CONDITIONALS

Peter M. Maurer (*maurer@csee.usf.edu*) - Univ. of Southern Florida, Tampa, FL

1B.2 OBSERVABILITY ANALYSIS OF EMBEDDED SOFTWARE FOR OVERAGE-DIRECTED VALIDATION

Jose Costa (*jccc@algos.inesc.pt*) - IST/INESC, Lisboa, Portugal
Srinivas Devadas - Massachusetts Institute of Technology, Cambridge, MA
Jose Monteiro - IST/INESC, Lisboa, Portugal

1B.3 A METHODOLOGY FOR VERIFYING MEMORY ACCESS PROTOCOLS IN BEHAVIORAL SYNTHESIS

Gernot Koch - Synopsys, Inc., Mountain View, CA
Taewhan Kim (*tkim@cs.kaist.ac.kr*) - KAIST, Taejon, Korea
Reiner Genevriere - Synopsys, Inc., Mountain View, CA

 - denotes videoed session

€ - denotes best paper

All Speakers are denoted in bold

Email Addresses are for corresponding authors

S - denotes short paper

Time: 11:00 AM to 12:30 PM Room: Donner/Siskiyou

METHODS FOR DSP SYNTHESIS AND DEBUGGING

Moderators: *Sridevan Parameswaran* - Univ. of Queensland, Brisbane, Australia
Kazutoshi Wakabayashi - NEC Corp., Kawasaki, Japan

This session presents three papers which improve DSP synthesis and debugging. The first paper deals with the symbolic debugging of DSP design. The second paper looks at estimating memory locations in DSP synthesis and the last paper deals with FIR filter multiplier optimization.

1C.1 SYMBOLIC DEBUGGING OF OPTIMIZED BEHAVIORAL SPECIFICATIONS

Darko Kirovski, Farinaz Koushanfar
(*farinaz@cs.ucla.edu*), *Miodrag Potkonjak* -
Univ. of California, Los Angeles, CA

1C.2 AUTOMATED DATA DEPENDENCY SIZE ESTIMATION WITH A PARTIALLY FIXED EXECUTION ORDERING

Per Gunnar Kjeldsberg
(*per.gunnar.kjeldsberg@fysef.ntnu.no*) - Norwegian
Univ. of Science/Technology, Trondheim, Norway
Francky Catthoor - IMEC, Leuven, Belgium
Einar J. Aas - Norwegian Univ. of Science/Technology,
Trondheim, Norway

1C.3 FIR FILTER SYNTHESIS ALGORITHMS FOR MINIMIZING THE DELAY AND THE NUMBER OF ADDERS

Hyeong-Ju Kang, Hansoo Kim, In-Cheol Park
(*icpark@bslab.kaist.ac.kr*) - KAIST, Taejon, Korea

Time: 11:00 AM to 12:30 PM Room: Oak

ISSUES IN TIMING ESTIMATION

Moderators: *Florentin Dartu* - Intel Corp., Hillsboro, OR
Anirudh Devgan - IBM Corp., Austin, TX

Timing estimation continues to be of high interest especially when combined with results from other areas. The first paper looks into interconnect optimization techniques as they influence timing and noise. The second one presents a timing analysis approach that considers intra-chip variations. The third paper covers a new method for miller factor computation.

1D.1 EFFECTS OF GLOBAL INTERCONNECT OPTIMIZATIONS ON PERFORMANCE ESTIMATION OF DEEP SUBMICRON DESIGNS

Andrew B. Kahng (*abk@cs.ucla.edu*) - Univ. of
California, Los Angeles, CA
Dennis Sylvester - Univ. of Michigan, Ann Arbor, MI
Dirk Stroobandt - Univ. of California, Los Angeles, CA
Sudhakar Muddu - Silicon Graphics Inc.,
Mountain View, CA
Yu Cao - Univ. of California, Berkeley, CA

1D.2 IMPACT OF SYSTEMATIC SPATIAL INTRA-CHIP GATE LENGTH VARIABILITY ON PERFORMANCE OF HIGH-SPEED DIGITAL CIRCUITS

Michael Orshansky (*omisha@eecs.berkeley.edu*) -
Univ. of California/eSilicon Corp., Berkeley, CA
Linda Milor - eSilicon Corp., Berkeley, CA
Pinhong Chen, Kurt Keutzer, Chenming Hu -
Univ. of California, Berkeley, CA

1D.3 MILLER FACTOR FOR GATE-LEVEL COUPLING DELAY CALCULATION

Pinhong Chen (*pinhong@eecs.berkeley.edu*) -
Univ. of California, Berkeley, CA
Desmond Kirkpatrick - Intel Corp., Hillsboro, OR
Kurt Keutzer - Univ. of California, Berkeley, CA

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Time: 2:00 PM to 3:30 PM

Room: Pine/Fir

EMBEDDED TUTORIAL:
COMMUNICATION DESIGNS:
SYSTEM SYNTHESIS CHALLENGES
AND OPPORTUNITIES

Moderator: *Ellen M. Sentovich* - Cadence Berkeley Labs.,
Berkeley, CA

Communication designs form the fastest growing segment of the semiconductor market. Both network processors and wireless chipsets have been attracting a great deal of attention, resources and efforts in market place and design community. However, CAD tools developers have been very slow in addressing challenges and opportunities in communication designs. The embedded tutorial will provide not only critical summary of the field, but, more importantly, aims to provide an impetus and starting information and references to CAD researchers and developers to initiate development of high level design tools for network processors and wireless systems. System design issues will be covered in detail. Network processor topics will cover four main architectural components of ultra high speed communication application specific and programmable systems: switching fabrics, routing functions, queue policies, control management hardware as well as system software and system-on-chip design issues for this type of applications will be addressed. In particular, on-chip bus proposals and challenges will be covered in detail. The second part will cover a mobile processor used in a great variety of portable embedded systems such as personal digital organizers (PDAs), smart cards, appliances (such as MP-3 players and cameras), laptops, smart badges, cellular phones, wearable computers, and sensor networks, and their shared and unique needs for low power, code density, security, cost sensitivity and multimedia and communication. Special emphasis will be given to software and pico radios, which are at the leading edge of the new wave of wireless communication revolution. Both research and market trends will be covered and needs for specific system and high-level tools analyzed.

PRESENTERS:

Jan M. Rabaey - Univ. of California, Berkeley, CA

Miodrag Potkonjak - Univ. of California,
Los Angeles, CA

Time: 2:00 PM to 3:30 PM

Room: Donner/Siskiyou

EMBEDDED TUTORIAL: CHALLENGES
IN PHYSICAL CHIP DESIGN

Moderator: *Georges Gielen* - Katholieke Univ.,
Leuven, Belgium

The tutorial consists of three parts. In the first part, some laws will be derived to show that traditional approaches to high performance data processing will become obsolete beyond repair within a few years, even if interconnect properties can be handled adequately. By that time, completely new styles and/or revolutionary changes in technology will be necessary to enable the required growth in complexity and performance. We will give an overview of what processing steps are to be developed to release chip development from its performance confinement. We will also describe a layout style, which will be almost forced upon us because of the laws derived at the beginning of this tutorial.

The second part will analyze two strategies for handling these new styles and technological capabilities. They are based on two completely different, almost opposite reactions to the challenges created in the first part. The decomposition of the design tasks and the statement of the sub-problems, some with strong algorithmic solutions, will deepen the understanding of what challenges design automation for layout synthesis is facing, and at the same time point to some of the inroads toward complete and adequate solutions.

The third part is about processors already realized in silicon, which use multiple layers of active components. It will demonstrate the effectiveness of some of the algorithms outlined in the second part, and be evidence of the enormous increase in potential enabled by the recent advances in producing silicon chips. Although the key technology step is merely "film transfer" and therefore only a first stage toward truly three-dimensional chip design, it provides a convincing argument for the adequacy of this answer for high performance after 2005.

PRESENTERS:

Paul Stravers - Philips Research, Eindhoven,
The Netherlands

Ralph H.J.M. Otten - Eindhoven University of Technology,
Eindhoven, The Netherlands

- denotes videoed session

€ - denotes best paper

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Time: 4:00 PM to 5:30 PM

Room: Cedar

TOPICS IN ROUTING

Moderators: *John Lillis* - Univ. of Illinois, Chicago, IL
Majid Sarrafzadeh - Univ. of California,
 Los Angeles, CA

The first paper in this session presents a general graph model for FPGA switch boxes which considers multi-pin nets. The second paper considers the interactions between congestion, timing and topology selection in global routing. The third paper proposes a multi-commodity flow approach to buffer planning. The fourth paper suggests the use of both maze routing and pattern routing to improve speed and predictability.

3A.1 GENERAL MODELS FOR OPTIMUM ARBITRARY-DIMENSION FPGA SWITCH BOX DESIGNS

Hongbing Fan - Univ. of Victoria, Victoria, Canada
Jiping Liu - The Univ. of Lethbridge,
 Lethbridge, Canada
Yu-Liang Wu (*ylw@cse.cuhk.edu.hk*) - Chinese Univ.
 of Hong Kong, Shatin, Hong Kong

3A.2 A TIMING-CONSTRAINED ALGORITHM FOR SIMULTANEOUS GLOBAL ROUTING OF MULTIPLE NETS

Jiang Hu, *Sachin S. Sapatnekar*
 (*sachin@mail.ece.umn.edu*) - Univ. of Minnesota,
 Minneapolis, MN

3A.3 PROBABLY GOOD GLOBAL BUFFERING USING AN AVAILABLE BUFFER BLOCK PLAN

Feodor Dragan, *Andrew B. Kahng* (*abk@cs.ucla.edu*) -
 Univ. of California, Los Angeles, CA
Ion Mandoiu - Georgia Institute of Technology,
 Atlanta, GA
Sudhakar Muddu - Silicon Graphics Inc.,
 Mountain View, CA
Alexander Zelikovsky - Georgia State Univ.,
 Atlanta, GA

3A.4 PREDICTABLE ROUTING

Ryan Kastner (*kastner@ece.nwu.edu*), *Elaheh*
Bozorgzadeh - Northwestern Univ., Evanston, IL
Majid Sarrafzadeh - Univ. of California,
 Los Angeles, CA

Time: 4:00 PM to 5:30 PM

Room: Pine/Fir

PARTIAL VERIFICATION TECHNIQUES

Moderators: *Andreas Kuehlmann* - Cadence Berkeley Labs.,
 Berkeley, CA
Yunshan Zhu - Synopsys, Inc., Mountain View, CA

This session presents three papers in the area of partial verification. The first paper describes a refinement technique for partitioned verification based on examining counter example traces. A combination of multiple verification methods to increase the capacity of semi-formal verification is presented in the second paper. The last paper describes an approach to enhance the verification coverage by transforming existing testbenches.

3B.1 COUNTER EXAMPLE-GUIDED CHOICE OF PROJECTIONS IN APPROXIMATE SYMBOLIC MODEL CHECKING

Shankar G. Govindaraju
 (*shankar@encore.stanford.edu*), *David L. Dill* -
 Stanford Univ., Stanford, CA

3B.2 SMART SIMULATION USING COLLABORATIVE FORMAL AND SIMULATION ENGINES

Pei-Hsin Ho (*pho@synopsys.com*) - Synopsys, Inc.,
 Beaverton, OR
Thomas R. Shiple - Synopsys, Inc.,
 Mountain View, CA
Kevin Harer, *James H. Kukula*, *Robert Damiano* -
 Synopsys, Inc., Beaverton, OR
Valeria M. Bertacco - Synopsys, Inc., Mountain View, CA
Jerry Taylor, *Jiang Long* - Synopsys, Inc.,
 Beaverton, OR

3B.3 SIMULATION COVERAGE ENHANCEMENT USING TEST STIMULUS TRANSFORMATION

C. Norris Ip (*ip@cadence.com*) - Cadence Berkeley
 Labs., Berkeley, CA

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Time: 4:00 PM to 5:30 PM

Room: Donner/Siskiyou

SCHEDULING AND COMPILATION FOR EMBEDDED SYSTEMS

Moderators: *Xiaobo (Sharon) Hu* - Univ. of Notre Dame,
Notre Dame, IN
Luciano Lavagno - Universita' di Udine,
Udine, Italy

This session deals with two important issues in the design of embedded systems. First an embedded tutorial describes advanced compilation techniques to generate VLIW cores and hardware accelerators for high performance applications such as multi-media. The second presentation describes a scheduling technique for data flow specifications in the presence of uncertainties in the environment.

3C.1 EMBEDDED TUTORIAL: HARDWARE COMPILATION FOR HIGH-PERFORMANCE EMBEDDED SYSTEMS

Vinod Kathail (kathail@hpl.hp.com) -
Hewlett-Packard Labs., Palo Alto, CA

3C.2 DYNAMIC RESPONSE TIME OPTIMIZATION FOR SDF GRAPHS

Dirk Ziegenbein (d.ziegenbein@tu-bs.de),
Jan Uerpmann - Technical Univ. of Braunschweig,
Braunschweig, Germany
Rolf Ernst - Tech. Univ. of Braunschweig,
Braunschweig, Germany

REGISTRATION HOURS

Sunday, November 5	5:00 PM to 8:00 PM
Monday, November 6	7:30 AM to 5:00 PM
Tuesday, November 7	7:30 AM to 5:00 PM
Wednesday, November 8	8:00 AM to 5:00 PM
Thursday, November 9	8:00 AM to 10:00 AM

Time: 4:00 PM to 5:30 PM

Room: Oak

INDUCTANCE AND FULL-WAVE ANALYSIS

Moderators: *Matton Kamon* - Microcosm Technologies, Inc.,
Cambridge, MA
Mustafa Celik - Monterey Design Systems, Inc.,
Sunnyvale, CA

In the near term, full-chip interconnect analysis will require fast yet accurate methods for inductance extraction, and in the far term, full-wave analysis. The first two papers in this session present methods for reaching full-chip inductance extraction. The final paper describes a method to significantly reduce the computation time of full-wave finite-difference electromagnetic analysis.

3D.1 FULL-CHIP, THREE-DIMENSIONAL, SHAPES-BASED RLC EXTRACTION

Kenneth L. Shepard (shepard@ee.columbia.edu) -
Columbia Univ., New York, NY
Dipak Sitaram - Cadence Design Systems, Inc.,
New Providence, NJ
Yu Zheng - Columbia Univ., New York, NY

3D.2 HOW TO EFFICIENTLY CAPTURE ON-CHIP INDUCTANCE EFFECT: INTRODUCING A NEW CIRCUIT ELEMENT K

Anirudh Devgan - IBM Corp., Austin, TX
Hao Ji (hji@cse.ucsc.edu), *Wayne W.M. Dai* -
Univ. of California, Santa Cruz, CA

3D.3 GENERALIZED FDTD-ADI: AN UNCONDITIONALLY STABLE FULL-WAVE MAXWELL'S EQUATIONS SOLVER FOR VLSI INTERCONNECT MODELING

Charlie C.-P. Chen (chen@enr.wisc.edu),
Tae-Woo Lee, *Narayanan Murugesan*,
Susan C. Hagness - Univ. of Wisconsin, Madison, WI

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Time: 9:00 AM to 10:30 AM

Room: Cedar

PLACEMENT I

Moderators: *Patrick Groeneveld* - Magma Design Automation, Inc., Cupertino, CA
Hidetoshi Onodera - Kyoto Univ., Kyoto, Japan

The first paper in this session on advanced placement issues describes a "hybrid" placer. It uses a global placement technique followed by a novel detailed placer. The second paper uses a different multi-level placement method that is applicable for large circuits. Finally, an improved macro-cell placer is presented.

4A.1 MONGREL: HYBRID TECHNIQUES FOR STANDARD CELL PLACEMENT

Sung-Woo Hur, *John Lillis* (*jlillis@eecs.uic.edu*) - Univ. of Illinois, Chicago, IL

4A.2 MULTILEVEL OPTIMIZATION FOR LARGE-SCALE CIRCUIT PLACEMENT

Tony Chan, *Jason Cong* (*cong@cs.ucla.edu*), *Tianming Kong*, *Joseph R. Shinnerl* - Univ. of California, Los Angeles, CA

4A.3 A FORCE-DIRECTED MACRO-CELL PLACER

Fan Mo (*fanmo@ic.eecs.berkeley.edu*), *Abdallah Tabbara*, *Robert K. Brayton* - Univ. of California, Berkeley, CA

PARTICIPATE IN THE
CONFERENCE SURVEY
AND WIN \$200

ICCAD would like you to voice your opinion on various aspects of the conference. ICCAD is conducting a survey in order to determine how to best serve your needs. Please complete the survey form and drop it off at the Registration Desk.

This is your chance to be a **WINNER!**

Time: 9:00 AM to 10:30 AM

Room: Pine/Fir

HIGH-LEVEL DESIGN TOOLS FOR ANALOG CIRCUITS

Moderators: *Henry Chang* - Cadence Design Systems, Inc., San Jose, CA
Rob A. Rutenbar - Carnegie Mellon Univ., Pittsburgh, PA

Useful techniques for the high-level design of delta-sigma modulators and analog continuous time filters are presented in this session. The first paper discusses a new verification technique for delta-sigma Converters, while the second one describes a complete synthesis system for these circuits. Finally, the third paper looks into the issue of power estimation of analog continuous time filters.

4B.1 VERIFICATION OF DELTA-SIGMA CONVERTERS USING ADAPTIVE REGRESSION MODELING

Jeongjin Roh (*roh@cerc.utexas.edu*), *Suresh Seshadri*, *Jacob A. Abraham* - Univ. of Texas, Austin, TX

4B.2 DAISY: A SIMULATION-BASED HIGH-LEVEL SYNTHESIS TOOL FOR DELTA-SIGMA MODULATORS

Kenneth Francken (*kenneth.francken@esat.kuleuven.ac.be*), *Georges Gielen* - Katholieke Univ., Leuven, Belgium

4B.3 ACTIF: A HIGH-LEVEL POWER ESTIMATION TOOL FOR ANALOG CONTINUOUS-TIME FILTERS

Erik Lauwers (*erik.lauwers@esat.kuleuven.ac.be*), *Georges Gielen* - Katholieke Univ., Leuven, Belgium

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Time: 9:00 AM to 10:30 AM

Room: Donner/Siskiyou

DELAY BUDGETING AND DISTRIBUTION

Moderators: *Peter A. Beere* - Univ. of Southern California, Los Angeles, CA
Rajeev Murgai - Fujitsu Labs. of America, Inc., Sunnyvale, CA

The first paper proposes a new metric for capturing the area optimization potential of a combinational circuit under delay constraints. Applications to gate sizing and placement problems are also presented. The second paper also considers the delay budgeting problem and formulates it as a mathematical program. The last paper studies interconnect models of three-dimensional circuit structures using stochastic models.

4C.1 POTENTIAL SLACK: AN EFFECTIVE METRIC OF COMBINATIONAL CIRCUIT PERFORMANCE

Chunhong Chen (*chen@ece.nwu.edu*), *Xiaojian Yang* - Northwestern Univ., Evanston, IL
Majid Sarrafzadeh - Univ. of California, Los Angeles, CA

4C.2 DELAY BUDGETING FOR A TIMING-CLOSURE-DRIVEN DESIGN METHOD

Chien-Chu Kuo, *Allen C.-H. Wu* (*chunghaw@cs.nthu.edu.tw*) - Tsing Hua Univ., Hsin-chu, Taiwan, ROC

4C.3 STOCHASTIC WIRE-LENGTH DISTRIBUTION AND DELAY DISTRIBUTION OF 3-DIMENSIONAL CIRCUITS

Rongtian Zhang, *Kaushik Roy* (*kaushik@ecn.purdue.edu*), *Cheng-Kok Koh*, *David B. Janes* - Purdue Univ., West Lafayette, IN



Time: 9:00 AM to 10:30 AM

Room: Oak

INTERCONNECT ANALYSIS

Moderators: *Mustafa Celik* - Monterey Design Systems, Inc., Sunnyvale, CA
Florentin Dartu - Intel Corp., Hillsboro, OR

The first paper proposes a new hierarchical equivalent circuit modeling methodology that efficiently captures long-range couplings. The second paper gives a third-order accurate, physically realizable circuit model for RLC interconnect trees. Last, a new analytic RC interconnect delay estimate is proposed which accurately captures resistive shielding in a manner analogous to effective capacitance calculations.

4D.1 HIERARCHICAL INTERCONNECT CIRCUIT MODELS

Michael W. Beattie (*beattie@ece.cmu.edu*), *Satrajit Gupta*, *Lawrence T. Pileggi* - Carnegie Mellon Univ., Pittsburgh, PA

4D.2 HURWITZ STABLE REDUCED ORDER MODELING FOR RLC INTERCONNECT TREE

Xiaodong Yang (*xdyang@cs.ucsd.edu*), *Chung-Kuan Cheng*, *Walter H. Ku* - Univ. of California at San Diego, La Jolla, CA
Robert J. Carragher - Fujitsu Labs. of America, Inc., Sunnyvale, CA

4D.3 ECM: AN "EFFECTIVE" CAPACITANCE BASED DELAY METRIC FOR RC INTERCONNECT

Chandramouli V. Kashyap (*chandra@austin.ibm.com*), *Charles J. Alpert*, *Anirudh Devgan* - IBM Corp., Austin, TX

- denotes videoed session

€ - denotes best paper

All Speakers are denoted in bold
 Email Addresses are for corresponding authors

S - denotes short paper

Time: 11:00 AM to 12:30 PM

Room: Pine/Fir

EMBEDDED TUTORIAL: INCREMENTAL CAD**Moderator:** *Georges Gielen* - Katholieke Univ.,
Leuven Belgium

Incremental modification and optimization in VLSI Computer-Aided Design (CAD) is of fundamental importance. Full understanding and focused participation in research and development in the area of incremental and dynamic would help us cope with the complexity of present day VLSI systems and facilitates concurrent optimization. Also, modifying existing tools to make them truly incremental can be very beneficial.

RTL synthesis is done without any physical information. Consequently, the gate-level netlist is produced with conservative assumptions, which often result in over designing and misprediction. New generation tools that integrate multiple physical variables (e.g., placement, net topology, clock tree generation, power routing, etc.) can look at the netlist with far more accurate physical information. This allows us to fix problems that could not be foreseen at the higher level (e.g., timing, congestion), and to further optimize the netlist for area or power. We will present a general framework for incremental synthesis at the physical level, including techniques such as place & size, remapping, and resynthesis.

PRESENTERS:*Olivier Coudert* - Monterey Design Systems, Inc.,
Sunnyvale, CA*Jason Cong* - Univ. of California, Los Angeles, CA*Majid Sarrafzadeh* - Univ. of California, Los Angeles, CA

Time: 11:00 AM to 12:30 PM

Room: Donner/Siskiyou

**EMBEDDED TUTORIAL:
DECOMPOSING MODEL CHECKING TASKS
USING THE ASSUME-GUARANTEE PARADIGM****Moderator:** *Andreas Kuehlmann* - Cadence Berkeley Labs.,
Berkeley, CA

In the formal verification of designs with very large state spaces, the model-checking task needs to be decomposed into subtasks of manageable complexity. It is natural to decompose the model-checking task following the component structure of the design. However, an individual component often does not satisfy its requirements unless the component is put into the right context, which constrains the inputs to the component. Thus, in order to verify each component individually, we need to make assumptions about its inputs, which are provided by the other components of the design. This reasoning is circular: component A is verified under the assumption that context B behaves correctly, and symmetrically, B is verified assuming the correctness of A. The assume-guarantee paradigm provides a systematic theory and methodology for ensuring the soundness of the circular style of postulating and discharging assumptions in component-based reasoning.

We give a tutorial introduction to the assume-guarantee paradigm by stepping in detail through the formal verification of a processor pipeline against an instruction set architecture. In this example, the verification of a three-stage pipeline is broken up into three subtasks, one for each stage of the pipeline.

PRESENTERS:*Thomas A. Henzinger* - Univ. of California, Berkeley, CA*Shaz Qadeer* - Compaq Systems Research Center,
Palo Alto, CA*Sriram Rajamani* - Microsoft Research, Redmond, WA - denotes videoed session

€ - denotes best paper

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S - denotes short paper

Time: 2:00 PM to 3:30 PM

Room: Cedar

PLACEMENT II

Moderators: *Jason Cong* - Univ. of California, Los Angeles, CA
Carl Sechen - Univ. of Washington, Seattle, WA

This session presents new techniques in VLSI placement, including partition-driven placement using simultaneous level partitioning and net-cut minimization formulation, as well as datapath placement with regularity.

6A.1 EFFECTIVE PARTITION-DRIVEN PLACEMENT WITH SIMULTANEOUS LEVEL PROCESSING AND GLOBAL NET VIEW

Ke Zhong, Shantanu Dutt (dutt@eecs.uic.edu) - Univ. of Illinois, Chicago, IL

6A.2 DRAGON2000: FAST STANDARD-CELL PLACEMENT FOR LARGE CIRCUITS

Maogang Wang (mgwang@ece.nwu.edu), Xiaojian Yang - Northwestern Univ., Evanston, IL
Majid Sarrafzadeh - Univ. of California, Los Angeles, CA

6A.3 DATA PATH PLACEMENT WITH REGULARITY

Terry Tao Ye (taoye@stanford.edu), Giovanni De Micheli - Stanford Univ., Stanford, CA

Time: 2:00 PM to 3:30 PM

Room: Pine/Fir

ANALOG AND RF SIMULATION

Moderators: *Koen Lampaert* - Conexant Systems, Inc., Newport Beach, CA
Ramesh Harjani - Univ. of Minnesota, Minneapolis, MN

This session offers new algorithms for steady-state and noise analysis of RF circuits and oscillators. The first paper presents new numerical methods for the mixed-frequency time formulation of quasi-periodic steady-state and small signal analysis. The second paper discusses noise analysis of phase-locked loops using stochastic differential equations. The session finishes with a new numerical method for evaluating phase noise in oscillators.

6B.1 EFFICIENT FINITE-DIFFERENCE METHOD FOR QUASI-PERIODIC STEADY-STATE AND SMALL SIGNAL ANALYSES

Baolin Yang (byang@cadence.com), Dan Feng, Joel R. Phillips, Keith Nabors, Kenneth S. Kundert - Cadence Design Systems, Inc., San Jose, CA

6B.2 NOISE ANALYSIS OF PHASE-LOCKED LOOPS

Amit Mehrotra (amehrotr@uivlsi.csl.uiuc.edu) - Univ. of Illinois, Urbana, IL

6B.3 COMPUTING PHASE NOISE EIGENFUNCTIONS DIRECTLY FROM STEADY-STATE JACOBIAN MATRICE

Alper Demir, David Long, Jaijeet S. Roychowdhury (jaijeet@research.bell-labs.com) - Bell Labs., Murray Hill, NJ

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Time: 2:00 PM to 3:30 PM

Room: Donner/Siskiyou

MARKOVIAN ANALYSIS AND ASYNCHRONOUS CIRCUITS

Moderators: *Steven M. Nowick* - Columbia Univ., New York, NY
Massoud Pedram - Univ. of Southern California,
Los Angeles, CA

The first paper in this session proposes the use of Markovian analysis to study the performance of clock and data recovery circuits. The second and third papers describe recent advances in asynchronous CAD, the first presenting new methods for architectural optimization and the second presenting a new method for fast logic synthesis.

6C.1 MODELING AND ANALYSIS OF COMMUNICATION CIRCUIT PERFORMANCE USING MARKOV CHAINS AND EFFICIENT GRAPH REPRESENTATIONS

Alper Demir (alpdemir@research.bell-labs.com),
Peter Feldmann - Bell Labs., Murray Hill, NJ

6C.2 PIPELINE OPTIMIZATION FOR ASYNCHRONOUS CIRCUITS: COMPLEXITY ANALYSIS AND AN EFFICIENT OPTIMAL ALGORITHM

Sangyun Kim (sangyunk@eiger.usc.edu), *Peter A.
Beerel* - Univ. of Southern California, Los Angeles, CA

6C.3 ACHIEVING FAST AND EXACT HAZARD-FREE LOGIC MINIMIZATION OF EXTENDED BURST-MODE GC FINITE STATE MACHINES

Hans Jacobson (hans@cs.utah.edu), *Chris J. Myers*,
Ganesh Gopalakrishnan - Univ. of Utah,
Salt Lake City, UT



Time: 2:00 PM to 3:30 PM

Room: Oak

LOW POWER INTERCONNECT MODELING AND OPTIMIZATION

Moderators: *Miodrag Potkonjak* - Univ. of California,
Los Angeles, CA
Kazutoshi Wakabayashi - NEC Corp.,
Kawasaki, Japan

The first paper introduces a new high-level graph-theoretic technique for power minimization in interconnect. The last two papers introduce a new paradigm for power minimization in interconnect which takes into account not only switching power, but also coupling capacitance effects. The paradigm is used to optimize power at the high level.

6D.1 BUS OPTIMIZATION FOR LOW-POWER DATA PATH SYNTHESIS BASED ON NETWORK FLOW METHOD

Sungpack Hong, *Taewhan Kim* (tkim@cs.kaist.ac.kr) -
KAIST, Taejeon, Korea

6D.2 COUPLING-DRIVEN SIGNAL ENCODING SCHEMES FOR LOW-POWER INTERFACE DESIGN

Ki-Wook Kim (kkim7@uiuc.edu), *Kwang-Hyun Baek*,
Naresh R. Shanbhag - Univ. of Illinois, Urbana, IL
C.L. Liu - National Tsing Hua Univ.,
Hsin-chu, Taiwan, ROC
Sung-Mo (Steve) Kang - Univ. of Illinois, Urbana, IL

6D.3 BUS ENERGY MINIMIZATION BY TRANSITION PATTERN CODING (TPC) IN DEEP SUB-MICRON TECHNOLOGIES

Paul-Peter Sotiriadis (pps@mit.edu),
Anantha Chandrakasan - Massachusetts
Institute of Technology, Cambridge, MA

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Time: 4:00 PM to 5:30 PM

Room: Gateway Ballroom

PANEL: WHY DOESN'T EDA
GET ENOUGH RESPECT?

Moderator: *A. Richard Newton - Univ. of California,
Berkeley, CA*

The success of EDA is a critical ingredient to the success of the semiconductor industry and to its many customers. But while semiconductor companies will spend billions on chip fabrication factories, there is a perception that funding for EDA is much less important. To be successful in EDA requires the brightest and broadest engineers, yet EDA company market caps and employee compensation, relative to other industry sectors that depend on EDA, do not seem to reflect this. What must we do in the EDA industry to get more respect and to break out of this unwelcome and ultimately destructive position? Must we recast the industry in an entirely different way? Should we work harder to demonstrate the true value of EDA as it is today? Or must we find ways to participate directly in the perceived value of our customers?

PANELISTS:

Andreas Bechtolsheim - CISCO Systems, Mountain View, CA

Joe Costello - think3 Inc., Santa Clara, CA

Aart De Geus - Synopsys, Inc., Mountain View, CA

Patrick Scaglia - Hewlett-Packard Labs., Palo Alto, CA

Jennifer Smith - Myriad Investments, Chestnut Hill, MA

Time: 9:00 AM to 10:30 AM

Room: Cedar

STATIC TIMING ANALYSIS

Moderators: *Sachin S. Sapatnekar* - Univ. of Minnesota, Minneapolis, MN
Timothy M. Burks - Magma Design Automation, Inc., Cupertino, CA

This session presents recent developments in the area of static timing analysis. The first paper examines the impact of crosstalk on delay, suggesting scheduling algorithms to compute switching windows. The second paper incorporates the effect of input slopes during static timing analysis, and the final presentation discusses a novel caching-based strategy using interpolation of cached data to speed up timing analysis.

8A.1 SWITCHING WINDOW COMPUTATION FOR STATIC TIMING ANALYSIS IN PRESENCE OF CROSSTALK NOISE

Pinhong Chen (*pinhong@eecs.berkeley.edu*) - Univ. of California, Berkeley, CA
Desmond Kirkpatrick - Intel Corp., Hillsboro, OR
Kurt Keutzer - Univ. of California, Berkeley, CA

8A.2 SLOPE PROPAGATION IN STATIC TIMING ANALYSIS

David Blaauw (*blaauw@advtools.sps.mot.com*),
Vladimir Zolotov, *Savithri Sundareswaran*, *Rajendran V. Panda*, *Chanhee Oh* - Motorola, Inc., Austin, TX

8A.3 TRANSISTOR-LEVEL TIMING ANALYSIS USING EMBEDDED SIMULATION

Pawan Kulshreshtha (*pawank@cadence.com*),
Robert Palermo, *Mohammad Mortazavi* - Cadence Design Systems, Inc., San Jose, CA
Cyrus Bamji - Canesta Inc., Santa Clara, CA
Hakan Yalcin - Cadence Design Systems, Inc., San Jose, CA

Time: 9:00 AM to 10:30 AM

Room: Pine/Fir

EMBEDDED SYSTEMS POWER MANAGEMENT AND VALIDATION

Moderators: *Felice Balarin* - Cadence Berkeley Labs., Berkeley, CA
Frank Vahid - Univ. of California, Riverside, CA

The first three papers deal with system-level power optimization. The first paper explores the issue of latency when power management is present. The next two papers propose process scheduling methods for variable voltage processors. The session ends with a paper that introduces a fault coverage metric for validating behavioral HDL descriptions.

8B.1 LATENCY EFFECTS OF POWER MANAGEMENT ALGORITHMS

Dinesh Ramanathan, *Sandy Irani*, *Rajesh K. Gupta* (*gupta@uci.edu*) - Univ. of California, Irvine, CA

8B.2 POWER-CONSCIOUS JOINT SCHEDULING OF PERIODIC TASK GRAPHS AND APERIODIC TASKS IN DISTRIBUTED REAL-TIME EMBEDDED SYSTEMS

Jiong Luo, *Niraj K. Jha* (*jha@ee.princeton.edu*) - Princeton Univ., Princeton, NJ

8B.3S POWER OPTIMIZATION OF REAL-TIME EMBEDDED SYSTEMS ON VARIABLE SPEED PROCESSORS

Youngsoo Shin (*ysshin@iis.u-tokyo.ac.jp*) - Univ. of Tokyo, Tokyo, Japan
Kiyoung Choi - Seoul National Univ., Seoul, Korea
Takayasu Sakurai - Univ. of Tokyo, Tokyo, Japan

8B.4S A DATA FLOW FAULT COVERAGE METRIC FOR VALIDATION OF BEHAVIORAL HDL DESCRIPTIONS

Qiushuang Zhang, *Ian G. Harris* (*harris@ecs.umass.edu*) - Univ. of Massachusetts, Amherst, MA

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€ - denotes best paper

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 Email Addresses are for corresponding authors

S - denotes short paper

Time: 9:00 AM to 10:30 AM

Room: Donner/Siskiyou

ADVANCES IN LAYOUT AND SYNTHESIS

Moderators: *Hamid Savoj* - Magma Design Automation, Inc.,
Cupertino, CA
Makoto Ikeda - Univ. of Tokyo,
Tokyo, Japan

This session presents recent advances in logic and layout optimizations. The first paper presents a mathematical programming approach to formulating and solving the problem of concurrent gate sizing and buffer insertion. The second paper addresses the problem of load and area constrained buffering of a single net whereas the third paper describes advances in synthesis of CMOS Domino logic to alleviate the charge sharing problem.

8C.1 SIMULTANEOUS GATE SIZING
AND FANOUT OPTIMIZATION

Wei Chen (*weich@sahand.usc.edu*) - Univ. of
Southern California, Los Angeles, CA
Cheng-Ta Hsieh - Verplex Systems, Inc., Milpitas, CA
Massoud Pedram - Univ. of Southern California,
Los Angeles, CA

8C.2 LAYOUT-DRIVEN AREA-CONSTRAINED TIMING
OPTIMIZATION BY NET BUFFERING

Rajeev Murgai (*murgai@fla.fujitsu.com*) -
Fujitsu Labs. of America, Inc., Sunnyvale, CA

8C.3 SYNTHESIS OF CMOS DOMINO CIRCUITS
FOR CHARGE SHARING ALLEVIATION

Ching-Hwa Cheng, *Shih-Chieh Chang*
(*scchang@cs.ccu.edu.tw*), *Shin-De Li*, *Jinn-Shyan*
Wang - National Chung-Cheng Univ., Chiayi,
Taiwan, ROC
Wen-Ben Jone - New Mexico Tech., Socorro, NM

Time: 9:00 AM to 10:30 AM

Room: Oak

EMBEDDED TUTORIAL
TEST OF FUTURE SoC

Moderator: *Rolf Ernst* - Technical Univ. Braunschweig,
Braunschweig, Germany

Spurred by technology leading to the availability of millions of gates per chip, system-level integration is evolving as a new paradigm, allowing entire systems to be built on a single chip. Being able to rapidly develop, manufacture, test, debug and verify complex SoCs is crucial for the continued success of the electronics industry. This growth is expected to continue full force at least for the next decade, while making possible the production of multimillion transistor chips. However, to make its production practical and cost effective, the industry road maps identify a number of major hurdles to be overcome. The key hurdle is related to test and diagnosis. This embedded tutorial analyzes these hurdles, relates them to the advancements in semiconductor technology and presents potential solutions to address them. These solutions are meant to ensure that test and diagnosis contribute to the overall growth of the SoC industry and do not slow it down. This embedded tutorial in addition presents the state-of-the-art in system-level integration and addresses the strategies and current industrial practices in the test of system-on-chip. It discusses the requirements for test reuse in hierarchical design, such as embedded test strategies for individual cores, test access mechanisms, optimizing test resource partitioning, and embedded test management and integration at the System-on-Chip level.

PRESENTERS:

Yervant Zorian - LogicVision Inc., San Jose, CA
Sujit Dey - Univ. of California at San Diego,
La Jolla, CA
Michael Rodgers - Intel Corp., Santa Clara, CA

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Time: 11:00 AM to 12:30 PM

Room: Cedar

NOISE AND PERFORMANCE ISSUES IN ROUTING

Moderators: *Tong Gao* - Monterey Design Systems, Inc.
Sunnyvale, CA
Margaret Marek-Sadowska - Univ. of California,
Santa Barbara, CA

This session addresses important performance issues in high performance designs. The first paper proposes a new useful skew tree algorithm for simultaneous skew scheduling and tree routing. The second paper proposes a novel twisted-bundle layout structure for minimizing inductive coupling noise. The third paper presents a design flow to alleviate the cross-talk problem by implementing logic as a network of PLAs using a dense wiring fabric which was proposed earlier.

9A.1 UST/DME: A CLOCK TREE ROUTER FOR GENERAL SKEW CONSTRAINTS

Chung-Wen Tsao - Ultima Interconnect Technology,
Sunnyvale, CA
Cheng-Kok Koh (*chengkoh@ecn.purdue.edu*) -
Purdue Univ., W. Lafayette, IN

9A.2 A TWISTED-BUNDLE LAYOUT STRUCTURE FOR MINIMIZING INDUCTIVE COUPLING NOISE

Guoan Zhong, *Haoran Wang*, *Cheng-Kok Koh*
(*chengkoh@ecn.purdue.edu*), *Kaushik Roy* -
Purdue Univ., West Lafayette, IN

9A.3 CROSS-TALK IMMUNE VLSI DESIGN USING A NETWORK OF PLAs EMBEDDED IN A REGULAR LAYOUT FABRIC

Sunil P. Khatri (*spkhatri@colorado.edu*) -
Univ. of Colorado, Boulder, CO
Robert K. Brayton, *Alberto L. Sangiovanni-Vincentelli* -
Univ. of California, Berkeley, CA

Time: 11:00 AM to 12:30 PM

Room: Pine/Fir

COMMUNICATION ARCHITECTURES DESIGN AND ANALYSIS

Moderators: *Diederik Verkest* - IMEC, Leuven, Belgium
Preeti Ranjan Panda - Synopsys, Inc.,
Mountain View, CA

This session deals with the design of communication architectures for system-on-chip, with the consideration of constraints in design space management, and with the analysis of the communication architectures to minimizing cache misses.

9B.1 LATENCY-GUIDED ON-CHIP BUS NETWORK DESIGN

Milenko Drinic, *Darko Kirovski* (*darko@cs.ucla.edu*) -
Univ. of California, Los Angeles, CA
Seapahn Meguerdichian - Univ. of California,
West Hills, CA
Miodrag Potkonjak - Univ. of California,
Los Angeles, CA

9B.2 EFFICIENT EXPLORATION OF THE SOC COMMUNICATION ARCHITECTURE DESIGN SPACE

Kanishka Lahiri (*klahiri@ece.ucsd.edu*) - Univ. of
California at San Diego, La Jolla, CA
Anand Raghunathan - NEC USA, C&C Research Labs.,
Princeton, NJ
Sujit Dey - Univ. of California at San Diego,
La Jolla, CA

9B.3 MIST: AN ALGORITHM FOR MEMORY MISS TRAFFIC MANAGEMENT

Peter Grun (*pgrun@ics.uci.edu*), *Nikil D. Dutt*,
Alex Nicolau - Univ. of California, Irvine, CA

 - denotes videoed session

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Email Addresses are for corresponding authors

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Time: 11:00 AM to 12:30 PM Room: Donner/Siskiyou

PERFORMANCE DRIVEN LOGIC SYNTHESIS

Moderators: *Shih-Chieh Chang* - National Chung-Cheng Univ., Chiayi, Taiwan, ROC
Masahiro Fujita - Univ. of Tokyo, Tokyo, Japan

The first paper addresses the issues that regularity may be destroyed during logic synthesis and proposes a mechanism to preserve regularity. The second paper focuses on the idea of gate duplication for timing optimization. The third paper shows a pseudo-polynomial time algorithm for gate assignment considering different rise and fall delays.

9C.1 REGULARITY DRIVEN LOGIC SYNTHESIS

Thomas Kutzschebauch
(*kutzsche@watson.ibm.com*), **Leon Stok** - IBM T.J. Watson Research Center, Yorktown Heights, NY

9C.2 TIMING DRIVEN GATE DUPLICATION: COMPLEXITY ISSUES AND ALGORITHMS

Ankur Srivastava (*ankur@ece.nwu.edu*), **Ryan Kastner** - Northwestern Univ., Evanston, IL
Majid Sarrafzadeh - Univ. of California, Los Angeles, CA

9C.3 AN EXACT GATE ASSIGNMENT ALGORITHM FOR TREE CIRCUITS UNDER RISE AND FALL DELAYS

Arlindo L. Oliveira - Cadence European Labs., Lisboa, Portugal
Rajeev Murgai (*murgai@fla.fujitsu.com*) - Fujitsu Labs. of America, Inc., Sunnyvale, CA

Time: 11:00 AM to 12:30 PM Room: Oak

NEW APPROACHES TO AT-SPEED BIST AND DIAGNOSIS

Moderators: *Yervant Zorian* - LogicVision, Inc., San Jose, CA
Sujit Dey - Univ. of California at San Diego, La Jolla, CA

At-Speed self-test and diagnosis are critical to high-quality manufacturing of next-generation ICs. This session presents two papers enabling at-speed BIST. The other two papers are on fault diagnosis of memory and programmable logic.

9D.1 IMPROVING THE PROPORTION OF AT-SPEED TESTS IN SCAN BIST

Yu Huang (*yhuang@eng.uiowa.edu*), **Irith Pomeranz**, **Sudhakar M. Reddy** - Univ. of Iowa, Iowa City, IA
Janusz Rajski - Mentor Graphics Corp., Wilsonville, OR

9D.2 FAST TEST APPLICATION TECHNIQUE WITHOUT FAST SCAN CLOCKS

Seonki Kim (*skkim@ece.umn.edu*), **Bapiraju Vinnakota** - Univ. of Minnesota, Minneapolis, MN

9D.3 ERROR CATCH AND ANALYSIS FOR SEMICONDUCTOR MEMORIES USING MARCH TESTS

Chi-Feng Wu, **Chih-Tsun Huang**, **Chih-Wea Wang**, **Kuo-Liang Cheng**, **Cheng-Wen Wu** (*cww@ee.nthu.edu.tw*) - National Tsing Hua Univ., Hsin-chu, Taiwan, ROC

9D.4 DIAGNOSIS OF INTERCONNECT FAULTS IN CLUSTER-BASED FPGA ARCHITECTURES

Ian G. Harris (*harris@ecs.umass.edu*), **Russell Tessier** - Univ. of Massachusetts, Amherst, MA

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Time: 2:00 PM to 3:30 PM

Room: Cedar

POWER ANALYSIS AND OPTIMIZATION

Moderators: *Dennis Sylvester* - Univ. of Michigan, Ann Arbor, MI
Anirudh Devgan - IBM Corp., Austin, TX

This session deals with power distribution and its effects. The first two papers present methods for analysis and optimization of power networks. The third paper provides a frequency-domain analysis technique for switching noise in power supply networks. The last paper proposes methods to improve dynamic timing analysis considering power supply noise effects.

10A.1 FAST ANALYSIS AND OPTIMIZATION OF POWER/GROUND NETWORKS

Haihua Su - Univ. of Minnesota, Minneapolis, MN
Kaushik Gala - Motorola, Inc., Austin, TX
Sachin S. Sapatnekar (*sachin@mail.ece.umn.edu*) - Univ. of Minnesota, Minneapolis, MN

10A.2S SIMULATION AND OPTIMIZATION OF THE POWER DISTRIBUTION NETWORK IN VLSI CIRCUITS

Geng Bai, *Sudhakar Bobba*, *Ibrahim N. Hajj* (*i-hajj@uiuc.edu* or *hajj@hawaii.csl.uiuc.edu*) - Univ. of Illinois, Urbana, IL

10A.3S FREQUENCY DOMAIN ANALYSIS OF SWITCHING NOISE ON POWER SUPPLY NETWORK

Shiyong Zhao, *Kaushik Roy* (*kaushik@ecn.purdue.edu*), *Cheng-Kok Koh* - Purdue Univ., West Lafayette, IN

10A.4 PATH SELECTION AND PATTERN GENERATION FOR DYNAMIC TIMING ANALYSIS CONSIDERING POWER SUPPLY NOISE EFFECTS

Jing-Jia Liou (*jjliou@bigbend.ece.ucsb.edu*), *Angela Krstic* - Univ. of California, Santa Barbara, CA
Yi-Min Jiang - Synopsys, Inc., Mountain View, CA
Kwang-Ting (Tim) Cheng - Univ. of California, Santa Barbara, CA



Time: 2:00 PM to 3:30 PM

Room: Pine/Fir

VLIW EXPLORATION AND DESIGN SYNTHESIS

Moderators: *Santanu Dutta* - Phillips, Sunnyvale, CA
Ali Dasdan - Synopsys, Inc., Mountain View, CA

The first two papers consider various aspects of optimizing VLIW architectures for power and performance. Both papers develop realistic models for modern VLIW processors. The third paper introduces a new design style for register-transfer models and a synthesis method that targets the design from applicative descriptions.

10B.1 POWER EXPLORATION FOR EMBEDDED VLIW ARCHITECTURES

Mariagiovanna Sami, *Donatella Sciuto*, *Cristina Silvano* (*silvano@elet.polimi.it*), *Vittorio Zaccaria* - Politecnico di Milano, Milan, Italy

€ 10B.2 EXPLORING PERFORMANCE TRADEOFFS FOR CLUSTERED VLIW ASIPS

Margarida Jacome (*jacome@ece.utexas.edu*), *Gustavo de Veciana*, *Victor Lapinskii* - Univ. of Texas, Austin, TX

10B.3 SYNTHESIS OF OPERATION-CENTRIC HARDWARE DESCRIPTIONS

James C. Hoe (*jhoe@ece.cmu.edu*) - Carnegie Mellon Univ., Pittsburgh, PA
Arvind - Massachusetts Institute of Technology, Cambridge, MA

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Time: 2:00 PM to 3:30 PM

Room: Donner/Siskiyou

FLEXIBILITY IN LOGIC SYNTHESIS

Moderator: *Yuji Kukimoto* - Monterey Design Systems, Inc., Sunnyvale, CA

A logic circuit at the gate level is restructured to meet area, timing and power constraints. Core algorithms to restructure a circuit are based on exploiting don't cares, extracting common expressions and detecting regularities, or rewiring the circuit. This session explores don't cares for multi-valued multi-level circuits, ATPG techniques for resynthesis and the appearance of symmetries in logic designs.

10C.1 DON'T CARES AND MULTI-VALUED LOGIC NETWORK MINIMIZATION

Yunjian Jiang (*wjiang@eecs.berkeley.edu*), *Robert K. Brayton* - Univ. of California, Berkeley, CA

10C.2 GENERALIZED SYMMETRIES IN BOOLEAN FUNCTIONS

Victor N. Kravets (*vkavets@eecs.umich.edu*), *Karem A. Sakallah* - Univ. of Michigan, Ann Arbor, MI

10C.3 WIRE RE-CONNECTIONS BASED ON IMPLICATION FLOW GRAPH

Shih-Chieh Chang (*scchang@cs.ccu.edu.tw*), *Zhong-Zhen Wu*, *He-Zhe Yu* - National Chung-Cheng Univ., Chiayi, Taiwan, ROC

Time: 2:00 PM to 3:30 PM

Room: Oak

DIGITAL AND ANALOG TEST GENERATION

Moderators: *Bapiraju Vinnakota* - Univ. of Minnesota, Minneapolis, MN
Seiji Kajihara - Kyushu Institute of Technology, Iizuka, Japan

The session covers different aspects of IC test generation, including digital, analog and mixed-signal test generation. The first three papers on digital test generation deal with sequential circuits, scan-based circuits and acyclic sequential circuits. The two papers on analog test generation deal with parametric and hard faults.

10D.1S DETERMINISTIC TEST PATTERN GENERATION TECHNIQUES FOR SEQUENTIAL CIRCUITS

Ilker Hamzaoglu (*aih002@email.mot.com*) - Motorola Inc., Schaumburg, IL
Janak H. Patel - Univ. of Illinois, Urbana, IL

10D.2S SIMULATION BASED TEST GENERATION FOR SCAN DESIGNS

Irith Pomeranz (*irith@eng.uiowa.edu*), *Sudhakar M. Reddy* - Univ. of Iowa, Iowa City, IA

10D.3 TEST GENERATION FOR ACYCLIC SEQUENTIAL CIRCUITS WITH HOLD REGISTERS

Tomoo Inoue (*tomoo@im.hiroshima-cu.ac.jp*) - Hiroshima City Univ., Hiroshima, Japan
Debesh Kumar Das - Jadavpur Univ., Calcutta, India
Chiiho Sano - Nara Institute of Science and Technology, Nara, Japan
Takahiro Mihara - Mitsubishi Electronic Control Software Corp., Kobe, Japan
Hideo Fujiwara - Nara Institute of Science and Technology, Nara, Japan

10D.4S A PARAMETRIC TEST METHOD FOR ANALOG COMPONENTS IN INTEGRATED MIXED-SIGNAL CIRCUITS

Michael Pronath (*mcp@eda.ei.tum.de*), *Volker Gloeckel*, *Helmut E. Graeb* - Technical Univ. of Munich, Munich, Germany

10D.5S PARTIAL SIMULATION-DRIVEN ATPG FOR DETECTION AND DIAGNOSIS OF FAULTS IN ANALOG CIRCUITS

Sudip Chakrabarti (*sudip@ece.gatech.edu*), *Abhijit Chatterjee* - Georgia Institute of Technology, Atlanta, GA

Time: 4:00 PM to 5:30 PM

Room: Donner/Siskiyou

**EMBEDDED TUTORIAL:
SYSTEM AND ARCHITECTURE-LEVEL
POWER REDUCTION FOR
MICROPROCESSOR-BASED COMMUNICATION
AND MULTI-MEDIA APPLICATIONS**

Moderator: *Francky Catthoor* - IMEC, Leuven, Belgium

Current microprocessor architectures become more and more dominated by the data access bottlenecks in the cache, system bus and main memory subsystems. These also have a major influence on the system (board-level) power consumption. In the booming domain of (largely embedded) cost-sensitive communication and multi-media applications, more and more implementations make use of microprocessor based platforms for flexibility reasons. However, in order to provide sufficiently high data throughput at reasonable power consumption for these demanding applications, novel solutions for the memory access and data transfer will have to be introduced. These will have to be situated both at the processor architecture and the algorithm/compiler level.

The crucial question we want to address in this embedded tutorial session is where one can expect these novel solutions to rely on. We will show that they will be based both on innovative processor architecture ideas and on novel approaches in the application compiler technology.

At the processor architecture side, previous work has focused on microarchitecture enhancements like intelligent management of cache hierarchies and additional buffers. But can this approach provide the memory performance necessary to feed the modern highly parallel microprocessors at a low power consumption? We will discuss alternative solutions.

At the side of the algorithm transformations and compilation technology for embedded data-dominated applications, much evolution is present. We will show that decisions made at this stage heavily influence the final outcome when the appropriate architectural issues of the embedded memories are correctly incorporated. This has to happen both at the ILP (instruction-level parallelism) compiler and in the preceding system compilation stages.

The session is mainly intended for architecture designers dealing with embedded processors at low power budgets, which include large amounts of memories, or for application designers which handle low power data-dominated applications. In addition, we also target (system-level) design tool developers and researchers who look at design methodologies and tools which can support this type of processor architecture and application design.

PRESENTERS:*Lode Nachtergaele* - IMEC, Leuven, Belgium*Vivek Tiwari* - Intel Corp., Santa Clara, CA*Nikil Dutt* - Univ. of California, Irvine, CA

Time: 4:00 PM to 5:30 PM

Room: Pine/Fir

**EMBEDDED TUTORIAL:
DESIGN-MANUFACTURING INTERFACE
FOR 0.13 MICRON AND BELOW**

Moderator: *Lawrence T. Pileggi* - Carnegie Mellon Univ., Pittsburgh, PA

This tutorial will present the requirements for the design-manufacturing interface for the upcoming generations of ULSI technologies. We will start by presenting an overview of trends in semiconductor industry: accelerated roadmap which leads to further miniaturization, the increasing role of manufacturing fluctuations, shrinking time to market, product complexity (including SOC) and the overall disaggregation of semiconductor industry (emergence of fabless companies and increasing role of foundries in manufacturing). Then we will discuss the present, isolated approach to process development, product design and manufacturing. We will illustrate the current practices by several examples of state-of-the-art Design For Manufacturability (DFM) approaches showing both the EDA tools and databases.

We will then propose requirements for the integrated approach to DFM which will include the following features:

- process characterization (including characterization vehicles) to identify the key yield loss reasons (systematic, parametric, random defects)
- abstraction of manufacturability/reliability design rules including sub-wavelength litho (OPC, PSM) and realistic worst-case files - cost modeling and forecasting.

These DFM interface capabilities will re-define the design flow and will pose new requirements on the EDA. They will enable much more predictive design synthesis and much more realistic verification of the system before its manufacturing. The next part of the tutorial will propose such a design flow utilizing this DFM interface. We will focus on the following:

- technology choice (forecasting of performance, yield, cost and ramp-up)
- constraint propagation to high-level synthesis system
- high level design decisions using technology abstraction (monolithic vs. 2.5D, choice of IP cores, etc.)
- estimation of timing, signal integrity, power statistical distributions
- circuit design optimization for SOC - including mixed-signal components (design centering, timing optimization)
- layout optimization (including model-based OPC).

We will conclude the tutorial by discussing the technical and organizational challenges that must be overcome to successfully implement the new design-manufacturing interface.

PRESENTER:*Andrzej J. Strojwas* - Carnegie Mellon Univ., Pittsburgh, PA

TUTORIAL 1

MODERN PHYSICAL DESIGN: ALGORITHM
TECHNOLOGY AND METHODOLOGY

Time: 9:00 AM to 5:00 PM

Room: Cedar

Speakers:

Andrew B. Kahng - Univ. of California, Los Angeles, CA
Majid Sarrafzadeh - Univ. of California, Los Angeles, CA
Stan Chow - AmmoCore Technology, Inc., San Jose, CA

Background: This tutorial covers "the latest word" in physical chip implementation methodology and PD algorithm technology, going into more "detail" than the previous edition of the tutorial. The target audience consists of system and circuit designers who would benefit from understanding tool capabilities in this arena, CAD engineers (both R&D and support), design project managers, and academic researchers. Familiarity with basic PD methodology is assumed.

Description: The first section reviews PD implications of the process technology and system design roadmaps. A generic chip planning and implementation methodology will help set context. A review of fundamental PD problem formulations and algorithms will concentrate on latest developments in RTL and gate-level partitioning, block and coarse placement, top-level interconnect planning and optimization, and cell-based place-and-route. We motivate needs for incremental optimization techniques, handling incomplete design data, and new tool interactions and concurrent optimizations.

The second section focuses on "upstream interactions", between traditional PD and floorplanning and logic synthesis. Approaches to achieving a convergent, predictable implementation flow will be reviewed. These center on alternate methodologies for prediction/predictability and estimation, e.g., budgeting-based planning, small blocks + wireplanning, layout-driven logic synthesis, constant-delay methodology, etc. Attention will be given to performance and signal integrity optimizations.

The third section focuses on interactions with parasitic estimation, delay calculation, timing/power/SI validations, and static timing/noise analyses and characterizations. We discuss requirements for tight analysis loops, reconciliation of data models, and speed/accuracy of delay and noise estimates.

The fourth section describes new links between traditional PD and polygon-level optimizations (layout enhancements for manufacturability, layout-on-the-fly or liquid layout, etc.). Such linkages are becoming dominant in high-end ASIC methodologies due to manufacturing yield and die cost considerations.

Last, we compare the half-dozen leading variants in convergent RTL-down methodology, and how they respectively make demands on PD. This taxonomy includes recent methodologies that exploit distributed or parallel computational platforms, or that creatively invoke commodity SP&R to achieve greater design productivity.

TUTORIAL 2

INTERCONNECT-CENTRIC DESIGN AND
ANALYSIS FOR ELECTRICAL INTEGRITY
IN SYSTEMS-ON-A-CHIP

Time: 9:00 AM to 5:00 PM

Room: Pine

Speakers:

Dennis Sylvester - Univ. of Michigan, Ann Arbor, MI
Kenneth Shepard - Columbia Univ., New York, NY
Sudhakar Muddu - Silicon Graphics Inc., Mountain View, CA

Background: With rising clock rates and scaling technology, it is becoming increasingly necessary to design and model a very complex on chip electrical environment dominated by wires. In this tutorial, we describe the latest design and analysis approaches to ensuring the electrical integrity of today's systems-on-a-chip, tackling emerging problems such as inductance, substrate coupling, and power-supply integrity. This tutorial is designed for a target audience consisting of VLSI designers, managers, CAD tool developers, R&D engineers, and academic researchers. The goal is to enable attendees to address key interconnect-centric issues including all aspects of signal integrity, inductive effects, and high-performance clock and power distribution.

Description: We begin by describing the design and analysis techniques for signal integrity in deep submicron designs. We introduce the overall design flow and fundamental theories and concepts of RC/RLC interconnect analysis. We discuss the effects of capacitive and inductive coupling on line delay and noise. Design techniques to minimize capacitance and inductance effects are explored. In terms of analysis, we describe interconnect macromodeling in a static noise analysis framework. We also focus on inductance estimation, extraction, and analysis.

The impact of environmental factors including variations in power supply voltage, temperature, and physical factors due to process variations also affect the cycle time and design robustness. Large die sizes and higher operating frequencies, coupled with large on-die variations at reduced device geometries, call for special consideration of this type of "noise".

We then consider power supply integrity analysis for systems-on-a-chip, including IR and Ldi/dt analysis with full consideration of decoupling capacitance, switching activity, and package models. Power distribution methodologies will be discussed. Substrate coupling is also becoming an important new design and analysis concern for mixed-signal designs. Substrate effects will be considered in the context of substrate noise analysis, latch-up and ESD analysis, RF device modeling, and high-frequency interconnect analysis (current returns through the substrate). In addition to analysis, we will also consider design techniques for limiting all of these coupling interactions.

We will survey various clock distribution approaches and the applicability for large SoC designs. We will compare approaches such as H-tree, mesh, grid for a typical design in terms of requirements including local/global skew, jitter, slew rates, power, buffer area, clock wiring resources, and shielding area. We will review the latest approaches for clock distribution networks including usage of de-skew units to reduce the clock skew.

Throughout the tutorial we will consider measurement techniques and structures for calibrating and characterizing the on-chip electrical environment with an emphasis on interconnect and substrate effects. This is important for technology characterization, yield analysis, and modeling validation.

TUTORIAL 3

SYMBOLIC MODEL CHECKING:
PRINCIPLES AND ADVANCED TECHNIQUES

Time: 9:00 AM to 5:00 PM

Room: Fir

Speakers:**Kenneth L. McMillan** - Cadence Berkeley, Labs., Berkeley, CA**Kavita Ravi** - Cadence Design Systems, Inc.,
New Providence, NJ**Fabio Somenzi** - Univ. of Colorado, Boulder, CO

Background: The increasing cost of verification has spurred interest in formal methods. Over the last few years equivalence checkers have become popular, and model checking has been successfully used in many projects. Formal methods can significantly increase productivity, but an understanding of their strengths and limitations is crucial for their effectiveness. This tutorial surveys the foundations of model checking, addresses modeling and performance issues, and presents recent algorithmic advances.

Description: The tutorial is divided in four parts. The first part quickly reviews formal verification techniques in general. It presents an overview of the various methods for sequential and combinational verification, with emphasis on sequential. The objective of this first part is to establish context and motivation. The second part is an introduction to model checking. It discusses the representation of hardware circuits for model checking, and the types of properties that are commonly verified with model checking. Safety and liveness properties are defined. Temporal logics are introduced as languages to specify properties. CTL, LTL, and CTL* are presented and contrasted. Automata as a specification formalism are also reviewed. The notions of similarity relation are discussed. The mu-calculus is then introduced as the "object-code" of the various specification mechanisms, and the model checking algorithms for CTL, LTL, and CTL* are formulated in terms of it. Implicit (symbolic) and explicit enumeration algorithms are discussed for model checking. Binary Decision Diagrams are reviewed. Their application to symbolic model checking is examined. The generation of witnesses and counter examples is discussed. The third part of the tutorial deals with abstraction (reduction) techniques—both manual and automated. It introduces the notions of compositional verification, abstract interpretations, and Assume/Guarantee reasoning. Several types of reduction are illustrated, including data domain reductions and symmetry reductions. The application of these techniques benefits from the support of a proof assistant, which is discussed. The fourth part of the tutorial discusses approximation-based modelchecking, semi-exhaustive techniques, and efficient fix point computation, examining the issues that are related to the capacity limits of current model checkers. Specialized techniques for invariant checking, including the representation of environmental constraints are addressed. The combination of BDDs and CNF SAT solvers for efficient model checking is discussed.

TUTORIAL 4

GAIN-BASED LOGIC SYNTHESIS

Time: 9:00 AM to 5:00 PM

Room: Oak

Speakers:**Prabhakar Kudva** - IBM T.J. Watson Research Ctr.,
Yorktown Heights, NY**David Kung** - IBM T.J. Watson Research Ctr.,
Yorktown Heights, NY**Ruchir Puri** - IBM T.J. Watson Research Ctr.,
Yorktown Heights, NY**Leon Stok** - IBM T.J. Watson Research Ctr.,
Yorktown Heights, NY

Background: There exists a large gap between full-custom design and standard ASIC design. Gigahertz micro-processors have been announced while most ASIC parts run at maximum speeds of around 200 Mhz. However, a significant part of this gap can be closed by using the appropriate libraries and synthesis techniques. The same techniques that allow us to synthesize all control logic for gigahertz micro-processors, also helps the time consuming design closure of large complex ASICs. This is especially the case, when decisions early in the process are mistargeted due to the use of misleading wireload models. Delay models parameterized by gain allow predictable pre-placement synthesis without wire-load models and a more rapid evaluation of the effect of changes on the timing, thereby speeding up the combined synthesis and placement process.

Description: Delay models parameterized by gain significantly enhance the design and timing closure problems we are seeing in today's complex standard cell design methodologies. To use these techniques most effectively the libraries, algorithms and methodology need to be adapted. We will address all three of these and tie them together in a coherent methodology that enhances the predictability of the timing closure process.

We will revisit the circuit basics of standard cells and the creation of static delay models with emphasis on the construction of gain-based delay models. Guidelines for designing practical libraries and their implications will be discussed as well as efficient algorithms for timing analysis, and area and load calculation.

Gain-based delay models open the opportunities to the construction of a different class of synthesis algorithms. Technology mapping in particular can benefit from the load-independence property of these models. Recent algorithms from the literature will be discussed. Buffering and fanout tree construction are other examples of algorithms that can be made much more predictable. Wire and gate sizing will be revisited and shown how they can be done in this environment.

Gain-based synthesis opens the opportunity to synthesize predictably without wire-load models. The actual sizing can be postponed until deep in the physical design phases, resulting in a more reliable timing information and better identification of timing critical regions. A methodology will be described that ties these together.

This tutorial is intended for designers to get an insight in circuits and libraries for which very efficient algorithms exist to synthesize them, for CAD-tool developers to understand state-of-the-art algorithms for rapid design closure on large designs and for their managers to get an insight in the applicability of gain-based synthesis techniques to their specific design problems.